Quad 12-Bit, 50/65 MSPS, Serial, LVDS 3 V A/D Converter

AD9229

FEATURES

- Four ADCs in one package
- Serial LVDS digital output data rates to 780 Mbps (ANSI-644)
- Data and frame clock outputs
- SNR = 69.5 dB (to Nyquist)
- Excellent linearity
  - DNL = ±0.3 LSB (typical)
  - INL = ±0.4 LSB (typical)
- 400 MHz full power analog bandwidth
- Power dissipation
  - 1,350 mW at 65 MSPS
  - 985 mW at 50 MSPS
- 1 V p-p to 2 V p-p input voltage range
- 3.0 V supply operation
- Power-down mode
- Digital test pattern enable for timing alignments

APPLICATIONS

- Digital beam forming systems for ultrasound
- Wireless and wired broadband communications
- Communication test equipment

FUNCTIONAL BLOCK DIAGRAM

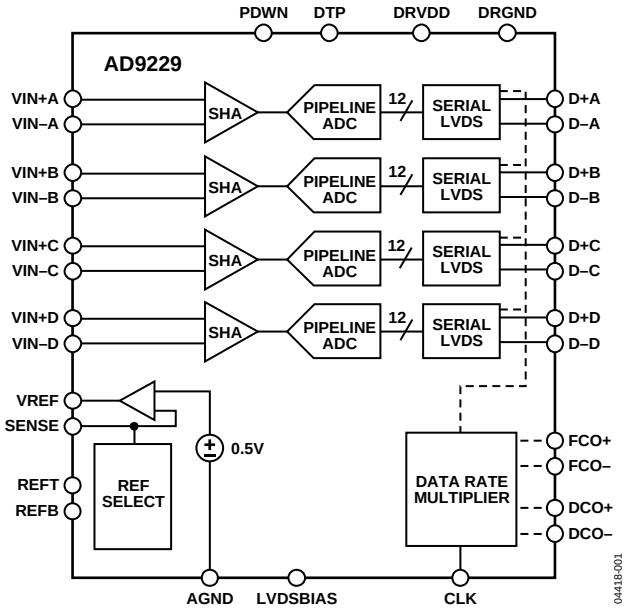

Figure 1.

PRODUCT DESCRIPTION

The AD9229 is a quad 12-bit, 65 MSPS analog-to-digital converter (ADC) with an on-chip sample-and-hold circuit that is designed for low cost, low power, small size, and ease of use. The product operates at up to a 65 MSPS conversion rate and is optimized for outstanding dynamic performance where a small package size is critical.

The ADC requires a single 3 V power supply and TTL-/CMOS-compatible sample rate clock for full performance operation. No external reference or driver components are required for many applications.

The ADC automatically multiplies the sample rate clock for the appropriate LVDS serial data rate. A data clock (DCO) for capturing data on the output and a frame clock (FCO) trigger for signaling a new output byte are provided. Power-down is supported and typically consumes 3 mW when enabled.

Fabricated with an advanced CMOS process, the AD9229 is available in a 48-lead LFCSP, Pb-free package. It is specified over the industrial temperature range of –40°C to +85°C.

PRODUCT HIGHLIGHTS

1. Four ADCs are contained in a small, space-saving package.
2. A data clock out (DCO) is provided, which operates up to 390 MHz and supports double-data rate operation (DDR).
3. The outputs of each ADC are serialized LVDS with data rates up to 780 Mbps (12 bits × 65 MSPS).
4. The AD9229 operates from a single 3.0 V power supply.
5. Packaged in a Pb-free, 48-lead LFCSP package.
6. The internal clock duty cycle stabilizer maintains performance over a wide range of input clock duty cycles.

Rev. 0

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REVISION HISTORY

3/05—Revision 0: Initial Version

SPECIFICATIONS

AVDD = 3.0 V, DRVDD = 3.0 V, maximum conversion rate, 2 V p-p differential input, 1.0 V internal reference, AIN = –0.5 dBFS, unless otherwise noted.

Table 1.

			AD9229-50			AD9229-65			
Parameter	**Temperature**	**Test Level**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION			12			12			Bits
ACCURACY									
No Missing Codes	Full	VI		Guaranteed			Guaranteed		
Offset Error	Full	VI		±5	±25		±5	±25	mV
Offset Matching	Full	VI		±5	±25		±5	±25	mV
Gain Error[1]	Full	VI		±0.3	±2.5		±0.3	±2.5	% FS
Gain Matching	Full	VI		±0.2	±1.5		±0.2	±1.5	% FS
Differential Nonlinearity (DNL)	25°C	V		±0.3			±0.3		LSB
	Full	VI		±0.3	±0.6		±0.3	±0.7	LSB
Integral Nonlinearity (INL)	25°C	V		±0.6			±0.4		LSB
	Full	VI		±0.6	±1		±0.4	±1	LSB
TEMPERATURE DRIFT									
Offset Error	Full	V		±2			±3		ppm/°C
Gain Error	Full	V		±12			±12		ppm/°C
Reference Voltage, VREF = 1 V	Full	V		±16			±16		ppm/°C
REFERENCE									
Output Voltage Error, VREF = 1 V	Full	VI		±10	±30		±10	±30	mV
Load Regulation @ 1.0 mA, VREF = 1 V	Full	V		3			3		mV
Output Voltage Error, VREF = 0.5 V	Full	VI		±8	±17		±8	±17	mV
Load Regulation @ 0.5 mA, VREF = 0.5 V	Full	V		0.2			0.2		mV
Input Resistance	Full	V		7			7		kΩ
ANALOG INPUTS									
Differential Input Voltage Range VREF = 1 V	Full	VI		2			2		V p-p
Differential Input Voltage Range VREF = 0.5 V	Full	VI		1			1		V p-p
Common Mode Voltage	Full	V		1.5			1.5		V
Input Capacitance	Full	V		7			7		pF
Analog Bandwidth, Full Power	Full	V		400			400		MHz
POWER SUPPLY									
AVDD	Full	IV	2.7	3.0	3.6	2.7	3.0	3.6	V
DRVDD	Full	IV	2.7	3.0	3.6	2.7	3.0	3.6	V
IAVDD	Full	VI		300	330		420	455	mA
DRVDD	Full	VI		28	31		29	33	mA
Power Dissipation[2]	Full	VI		985	1083		1350	1465	mW
Power-Down Dissipation	Full	V		3			3		mW
CROSSTALK[3]	Full	V		–95			–95		dB

[1] Gain error and gain temperature coefficients are based on the ADC only (with a fixed 1.0 V external reference and a 2 V p-p differential analog input).
[2] Power dissipation measured with rated encode and 2.4 MHz analog input at –0.5 dBFS.
[3] Typical specification over the first Nyquist zone.

AC SPECIFICATIONS

AVDD = 3.0 V, DRVDD = 3.0 V, maximum conversion rate, 2 V p-p differential input, 1.0 V internal reference, AIN = –0.5 dBFS, unless otherwise noted.

Table 2.

Parameter		Temperature	Test Level	AD9229-50			AD9229-65			Unit
				Min	Typ	Max	Min	Typ	Max	
SIGNAL-TO-NOISE RATIO (SNR)	f_{IN} = 2.4 MHz	Full	IV	69.5	70.4		69.0	70.2		dB
	f_{IN} = 10.3 MHz	25°C	V		70.4			70.2		dB
	f_{IN} = 25 MHz	Full	VI	68.7	69.6					dB
	f_{IN} = 30 MHz	Full	VI				68.0	69.5		dB
	f_{IN} = 70 MHz	25°C	V		67.2			67.1		dB
SIGNAL-TO-NOISE RATIO (SINAD)	f_{IN} = 2.4 MHz	Full	V		70.0			69.8		dB
	f_{IN} = 10.3 MHz	25°C	V		70.0			69.8		dB
	f_{IN} = 25 MHz	Full	VI	68.4	69.4					dB
	f_{IN} = 30 MHz	Full	VI				67.3	69.0		dB
	f_{IN} = 70 MHz	25°C	V		66.8			66.7		dB
EFFECTIVE NUMBER OF BITS (ENOB)	f_{IN} = 2.4 MHz	Full	V		11.3			11.3		Bits
	f_{IN} = 10.3 MHz	25°C	V		11.3			11.3		Bits
	f_{IN} = 25 MHz	Full	VI	11.1	11.2					Bits
	f_{IN} = 30 MHz	Full	VI				10.9	11.2		Bits
	f_{IN} = 70 MHz	25°C	V		10.8			10.8		Bits
SPURIOUS-FREE DYNAMIC RANGE (SFDR)	f_{IN} = 2.4 MHz	Full	V		85			85		dBc
	f_{IN} = 10.3 MHz	25°C	V		85			85		dBc
	f_{IN} = 25 MHz	Full	VI	76	85					dBc
	f_{IN} = 30 MHz	Full	VI				73	85		dBc
	f_{IN} = 70 MHz	25°C	V		78			77		dBc
WORST HARMONIC	f_{IN} = 2.4 MHz	Full	V		–85			–85		dBc
(Second or Third)	f_{IN} = 10.3 MHz	25°C	V		–85			–85		dBc
	f_{IN} = 25 MHz	Full	VI		–85	–76				dBc
	f_{IN} = 30 MHz	Full	VI					–85	–73	dBc
	f_{IN} = 70 MHz	25°C	V		–78			–77		dBc
WORST OTHER	f_{IN} = 2.4 MHz	Full	V		–90			–90		dBc
(Excluding Second or Third)	f_{IN} = 10.3 MHz	25°C	V		–90			–90		dBc
	f_{IN} = 25 MHz	Full	VI		–88	–81.7				dBc
	f_{IN} = 30 MHz	Full	VI					–88	–79.7	dBc
	f_{IN} = 70 MHz	25°C	V		–85			–83		dBc
TWO TONE INTERMOD ULATION DISTORTION (IMD) AIN1 and AIN2 = –7.0 dBFS	f_{IN1} = 15 MHz, f_{IN2} = 16 MHz	25°C	V		–73			–73		dBc
	f_{IN1} = 69 MHz, f_{IN2} = 70 MHz	25°C	V		–68.5			–68.5		dBc

DIGITAL SPECIFICATIONS

AVDD = 3.0 V, DRVDD = 3.0 V, maximum conversion rate, 2 V p-p differential input, 1.0 V internal reference, AIN = –0.5 dBFS, unless otherwise noted.

Table 3.

			AD9229-50			AD9229-65			
Parameter	**Temperature**	**Test Level**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
CLOCK INPUT									
Logic Compliance			TTL/CMOS			TTL/CMOS			
High Level Input Voltage	Full	IV	2.0			2.0			V
Low Level Input Voltage	Full	IV			0.8			0.8	V
High Level Input Current	Full	VI		0.5	±10		0.5	±10	µA
Low Level Input Current	Full	VI		0.5	±10		0.5	±10	µA
Input Capacitance	25°C	V		2			2		pF
LOGIC INPUTS (PDWN)									
Logic 1 Voltage	Full	IV	2.0			2.0			V
Logic 0 Voltage	Full	IV			0.8			0.8	V
High Level Input Current	Full	IV		0.5	±10		0.5	±10	µA
Low Level Input Current	Full	IV		0.5	±10		0.5	±10	µA
Input Capacitance	25°C	V		2			2		pF
DIGITAL OUTPUTS (D+, D–)									
Logic Compliance			LVDS			LVDS			
Differential Output Voltage	Full	VI	260		440	260		440	mV
Output Offset Voltage	Full	VI	1.15	1.25	1.35	1.15	1.25	1.35	V
Output Coding	Full	VI		Offset Binary			Offset Binary		

SWITCHING SPECIFICATIONS

AVDD = 3.0 V, DRVDD = 3.0 V, maximum conversion rate, 2 V p-p differential input, 1.0 V internal reference, AIN = –0.5 dBFS, unless otherwise noted.

Table 4.

			AD9229-50			AD9229-65			
Parameter	**Temp**	**Test Level**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
CLOCK									
Maximum Clock Rate	Full	VI	50			65			MSPS
Minimum Clock Rate	Full	IV			10			10	MSPS
Clock Pulse Width High (t_{EH})	Full	VI	8	10		6.2	7.7		ns
Clock Pulse Width Low (t_{EL})	Full	VI	8	10		6.2	7.7		ns
OUTPUT PARAMETERS									
Propagation Delay (t_{PD})	Full	VI	3.3	6.5	7.9	3.3	6.5	7.9	ns
Rise Time (t_R) (20% to 80%)	Full	V		250			250		ps
Fall Time (t_F) (20% to 80%)	Full	V		250			250		ps
FCO Propagation Delay (t_{FCO})	Full	V		6.5			6.5		ns
DCO Propagation Delay (t_{CPD})	Full	V		t_{FCO} + (t_{SAMPLE}/24)			t_{FCO} + (t_{SAMPLE}/24)		ns
DCO-to-Data Delay (t_{DATA})	Full	IV	(t_{SAMPLE}/24) – 250	(t_{SAMPLE}/24)	(t_{SAMPLE}/24) + 250	(t_{SAMPLE}/24) – 250	(t_{SAMPLE}/24)	(t_{SAMPLE}/24) + 250	ps
DCO-to-FCO Delay (t_{FRAME})	Full	IV	(t_{SAMPLE}/24) – 250	(t_{SAMPLE}/24)	(t_{SAMPLE}/24) + 250	(t_{SAMPLE}/24) – 250	(t_{SAMPLE}/24)	(t_{SAMPLE}/24) + 250	ps
Data-to-Data Skew ($t_{DATA-MAX}$ – $t_{DATA-MIN}$)	Full	IV		±100	±250		±100	±250	ps
Wake-Up Time	25°C	V		4			4		ms
Pipeline Latency	Full	IV		10			10		CLK cycles
APERTURE									
Aperture Delay (t_A)	25°C	V		1.8			1.8		ns
Aperture Uncertainty (Jitter)	25°C	V		<1			<1		ps rms
OUT-OF-RANGE RECOVERY TIME	25°C	V		2			2		CLK cycles

TIMING DIAGRAM

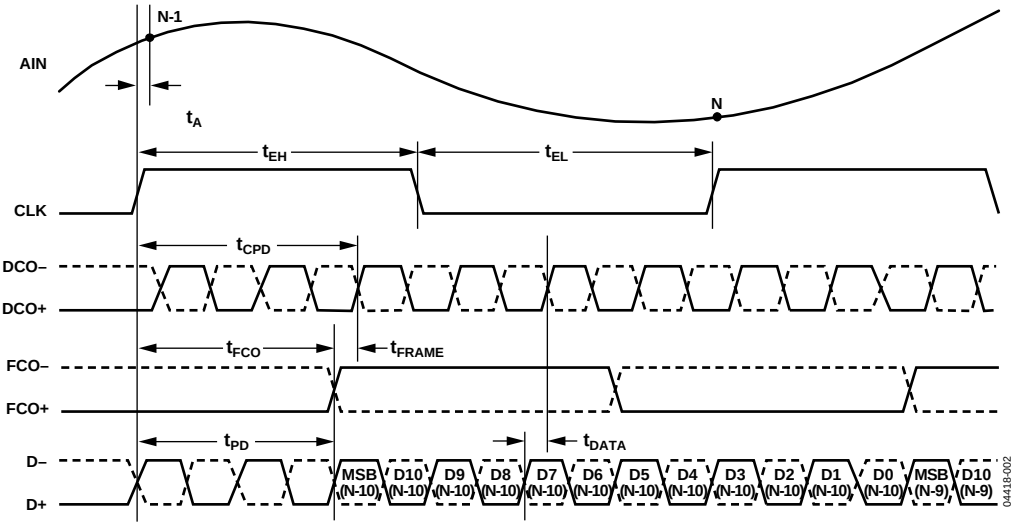

Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	With Respect To	Min	Max	Unit
ELECTRICAL				
AVDD	AGND	–0.3	+3.9	V
DRVDD	DRGND	–0.3	+3.9	V
AGND	DRGND	–0.3	+0.3	V
AVDD	DRVDD	–3.9	+3.9	V
Digital Outputs (D+, D–, DCO+, DCO–, FCO+, FCO–)	DRGND	–0.3	DRVDD	V
LVDSBIAS	DRGND	–0.3	DRVDD	V
CLK	AGND	–0.3	AVDD	V
VIN+, VIN–	AGND	–0.3	AVDD	V
PDWN, DTP	AGND	–0.3	AVDD	V
REFT, REFB	AGND	–0.3	AVDD	V
VREF, SENSE	AGND	–0.3	AVDD	V
ENVIRONMENTAL				
Operating Temperature Range (Ambient)		–40	+85	°C
Maximum Junction Temperature			150	°C
Lead Temperature (Soldering, 10 sec)			300	°C
Storage Temperature Range (Ambient)		–65	+150	°C
Thermal Impedance[1]			25	°C/W

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

EXPLANATION OF TEST LEVELS

I. 100% production tested.

II. 100% production tested at 25°C and guaranteed by design and characterization at specified temperatures.

III. Sample tested only.

IV. Parameter is guaranteed by design and characterization testing.

V. Parameter is a typical value only.

VI. 100% production tested at 25°C and guaranteed by design and characterization for industrial temperature range.

[1] θ_{JA} for a 4-layer PCB with solid ground plane in still air.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

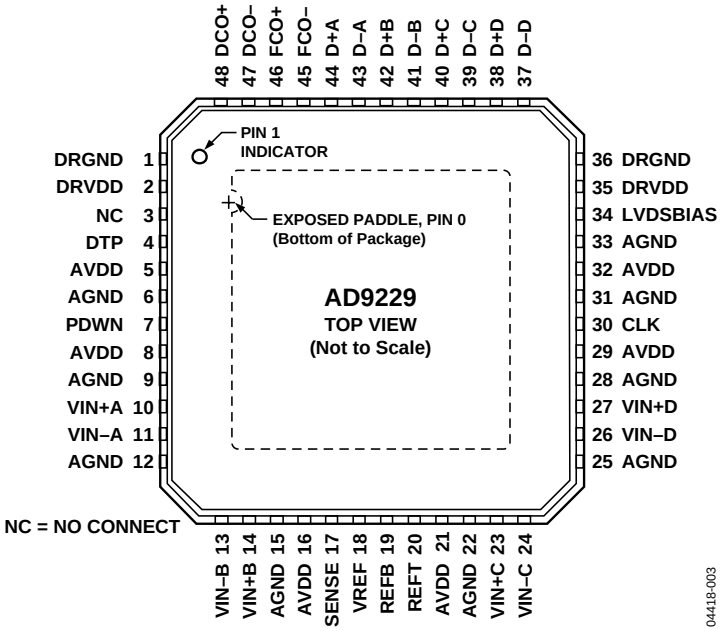

Figure 3. CSP Top View

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
5, 8, 16, 21, 29, 32	AVDD	Analog Supply
6, 9, 12, 15, 22, 25, 28, 31, 33	AGND	Analog Ground
2, 35	DRVDD	Digital Output Supply
1, 36	DRGND	Digital Ground
0	AGND	Exposed Paddle/Thermal Heat Slug (Located on Bottom of Package)
3	NC	No Connect
4	DTP	Digital Test Pattern Enable
7	PDWN	Power-Down Selection (AVDD = Power Down)
10	VIN+A	ADC A Analog Input—True
11	VIN–A	ADC A Analog Input—Complement
13	VIN–B	ADC B Analog Input—Complement
14	VIN+B	ADC B Analog Input—True
17	SENSE	Reference Mode Selection
18	VREF	Voltage Reference Input/Output
19	REFB	Differential Reference (Bottom)
20	REFT	Differential Reference (Top)
23	VIN+C	ADC C Analog Input—True
24	VIN–C	ADC C Analog Input—Complement
26	VIN–D	ADC D Analog Input—Complement
27	VIN+D	ADC D Analog Input—True
30	CLK	Input Clock
34	LVDSBIAS	LVDS Output Current Set Resistor Pin
37	D–D	ADC D Complement Digital Output
38	D+D	ADC D True Digital Output
39	D–C	ADC C Complement Digital Output
40	D+C	ADC C True Digital Output
41	D–B	ADC B Complement Digital Output
42	D+B	ADC B True Digital Output
43	D–A	ADC A Complement Digital Output
44	D+A	ADC A True Digital Output
45	FCO–	Frame Clock Indicator—Complement Output
46	FCO+	Frame Clock Indicator—True Output
47	DCO–	Data Clock Output—Complement
48	DCO+	Data Clock Output—True

EQUIVALENT CIRCUITS

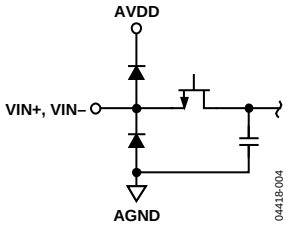

Figure 4. Equivalent Analog Input Circuit

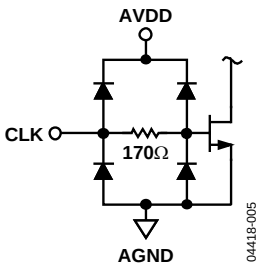

Figure 5. Equivalent Clock Input Circuit

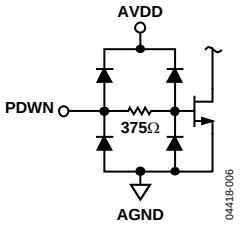

Figure 6. Equivalent Digital Input Circuit

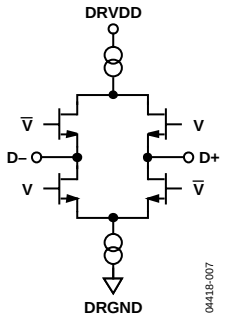

Figure 7. Equivalent Digital Output Circuit

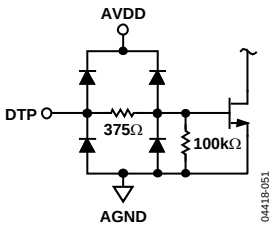

Figure 8. Equivalent DTP Input Circuit

TYPICAL PERFORMANCE CHARACTERISTICS

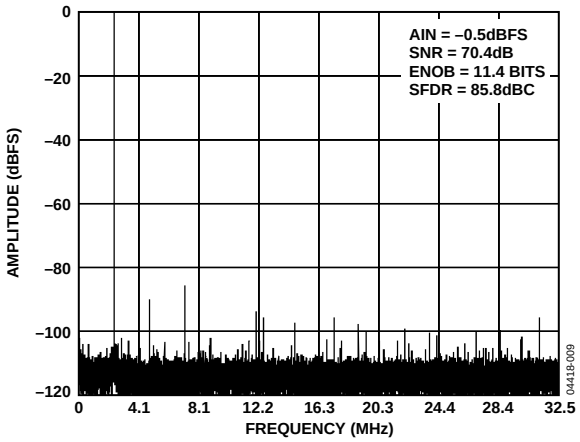

Figure 9. Single-Tone 32k FFT With f_{IN} = 2.4 MHz, f_{SAMPLE} = 65 MSPS

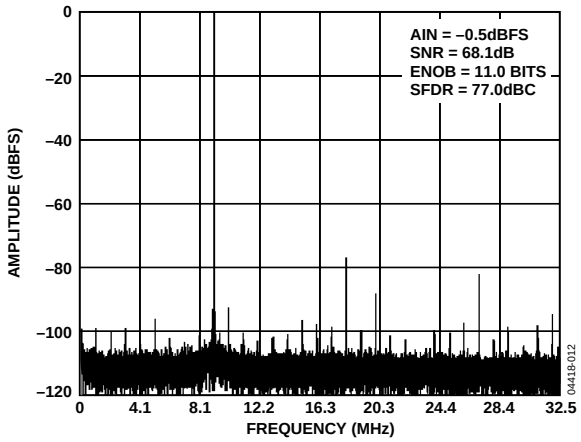

Figure 12. Single-Tone 32k FFT With f_{IN} = 120 MHz, f_{SAMPLE} = 65 MSPS

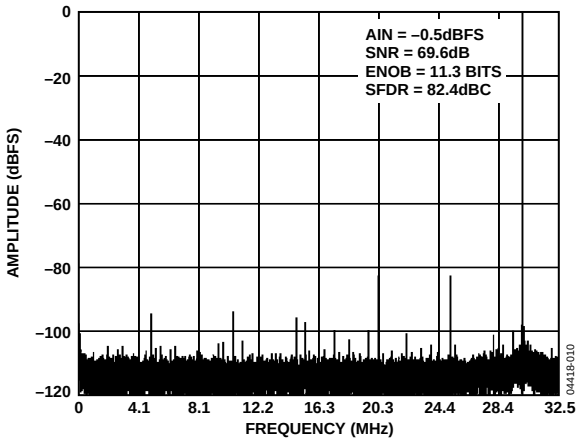

Figure 10. Single-Tone 32k FFT With f_{IN} = 30 MHz, f_{SAMPLE} = 65 MSPS

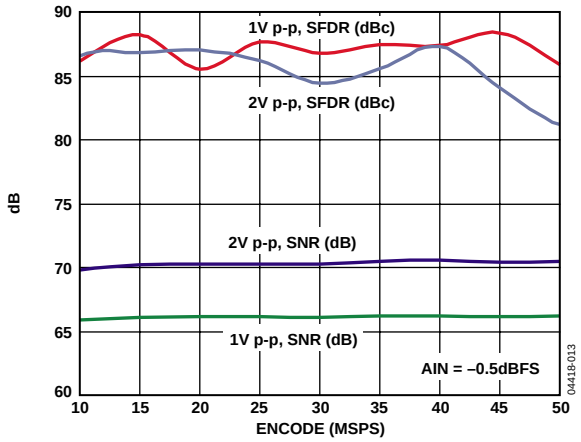

Figure 13. AD9229-50, SNR/SFDR vs. f_{SAMPLE}, f_{IN} = 10.3 MHz

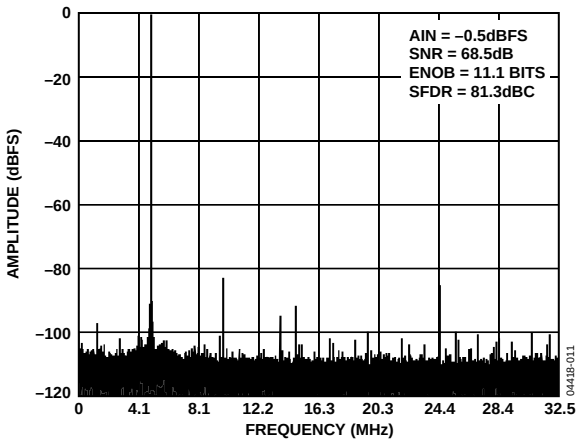

Figure 11. Single-Tone 32k FFT With f_{IN} = 70 MHz, f_{SAMPLE} = 65 MSP

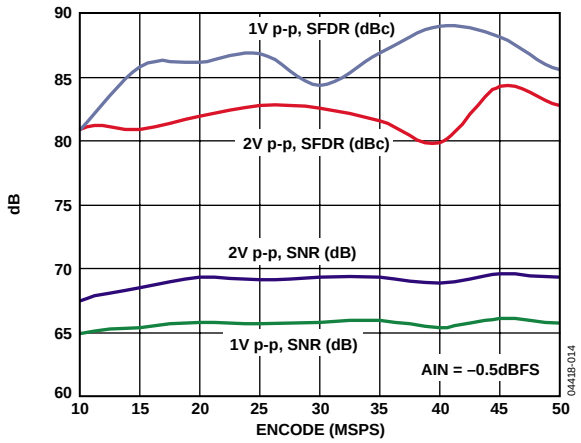

Figure 14. AD9229-50, SNR/SFDR vs. f_{SAMPLE}, f_{IN} = 25 MHz

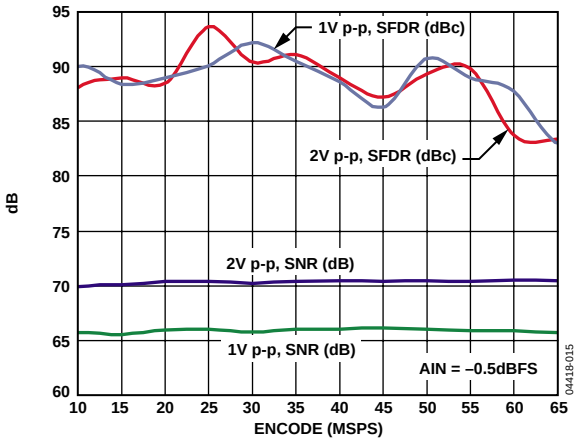

Figure 15. AD9229-65, SNR/SFDR vs. f_{SAMPLE}, f_{IN} = 10.3 MHz

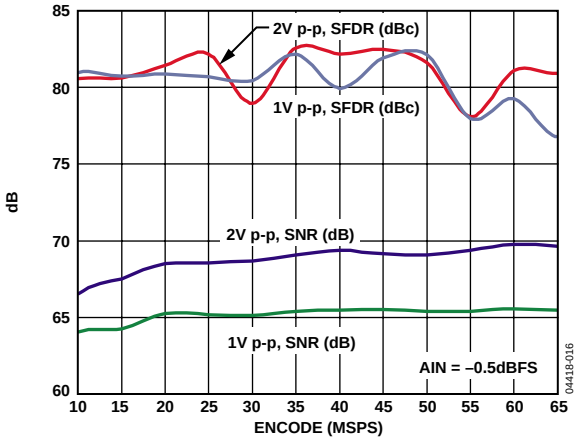

Figure 16. AD9229-65, SNR/SFDR vs. f_{SAMPLE}, f_{IN} = 30 MHz

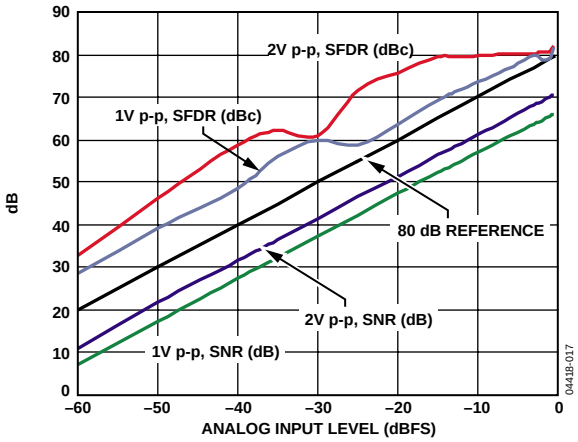

Figure 17. AD9229-50, SNR/SFDR vs. Analog Input Level, f_{IN} = 10.3 MHz

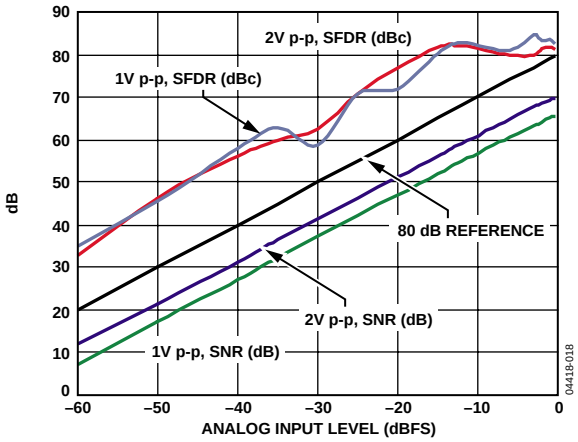

Figure 18. AD9229-50, SNR/SFDR vs. Analog Input Level, f_{IN} =25 MHz

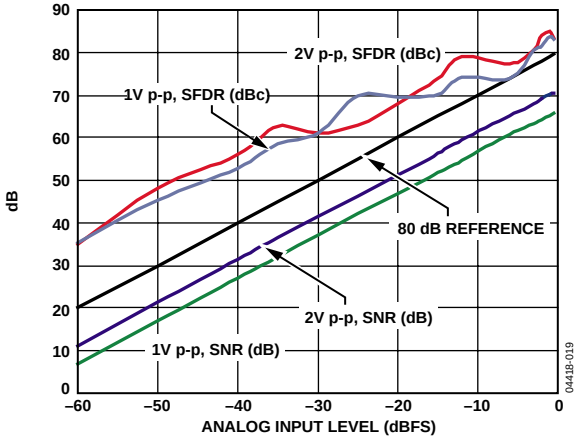

Figure 19. AD9229-65, SNR/SFDR vs. Analog Input Level, f_{IN} = 10.3 MHz

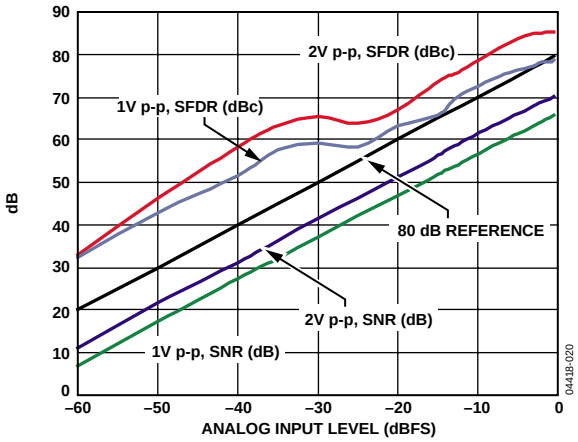

Figure 20. AD9229-65, SNR/SFDR vs. Analog Input Level, f_{IN} = 30 MHz

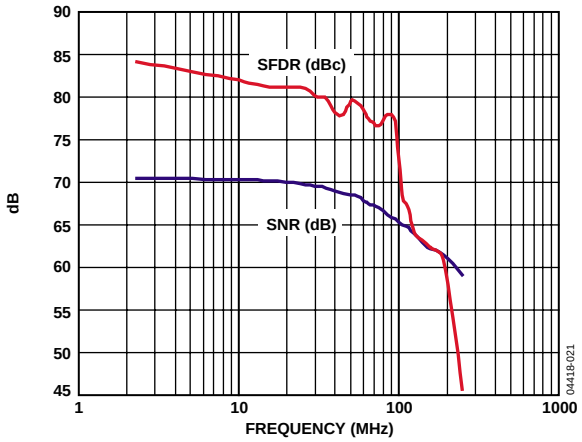

Figure 21. SNR/SFDR vs. f_{IN}, f_{SAMPLE} = 65 MHz

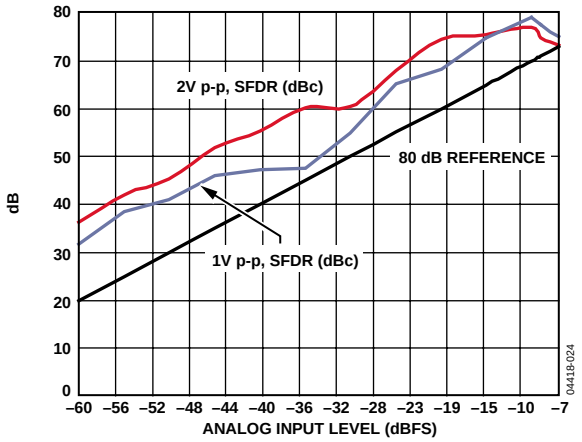

Figure 24. Two-Tone SFDR vs. Analog Input Level, f_{IN1} = 15 MHz and f_{IN2} = 16 MHz, f_{SAMPLE} = 65 MSPS

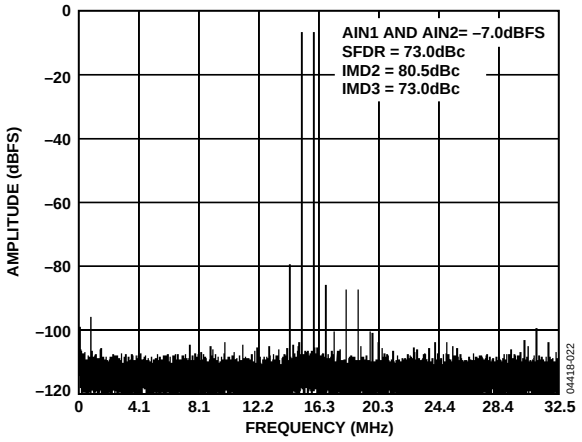

Figure 22. Two-Tone 32k FFT with f_{IN1} = 15 MHz and f_{IN2} = 16 MHz, f_{SAMPLE} = 65 MSPS

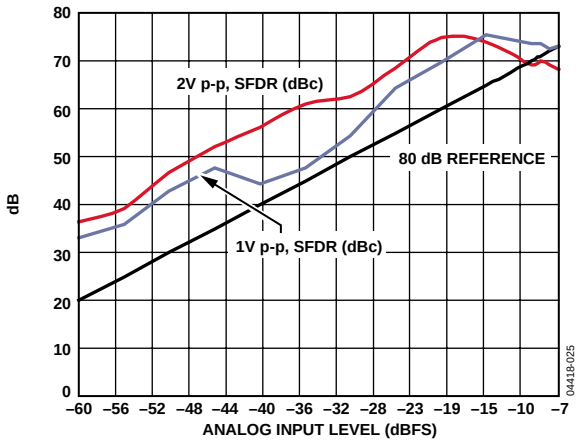

Figure 25. Two-Tone SFDR vs. Analog Input Level, f_{IN1} = 69 MHz and f_{IN2} = 70 MHz, f_{SAMPLE} = 65 MSPS

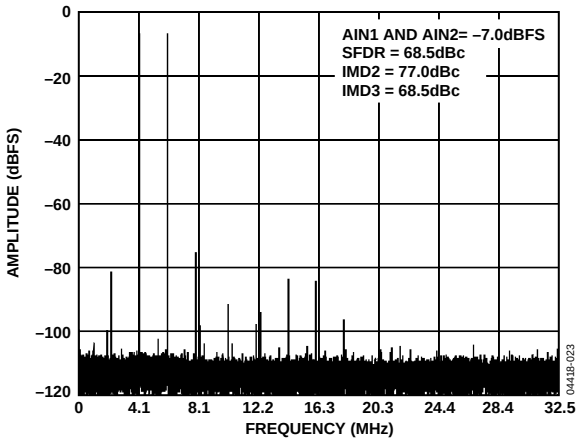

Figure 23. Two-Tone 32k FFT with f_{IN1} = 69 MHz and f_{IN2} = 70 MHz, f_{SAMPLE} = 65 MSPS

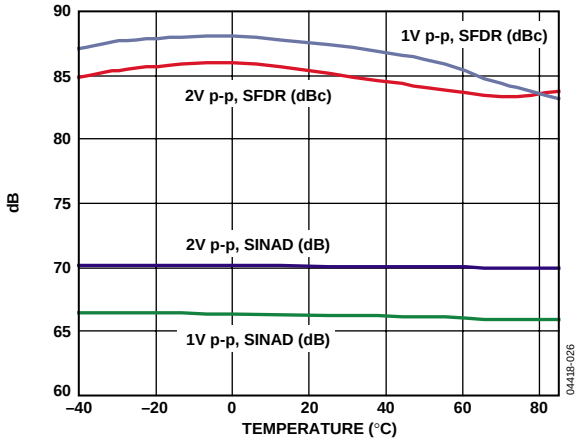

Figure 26. SINAD/SFDR vs. Temperature, f_{IN} 10.3 MHz, f_{SAMPLE} = 65 MSPS

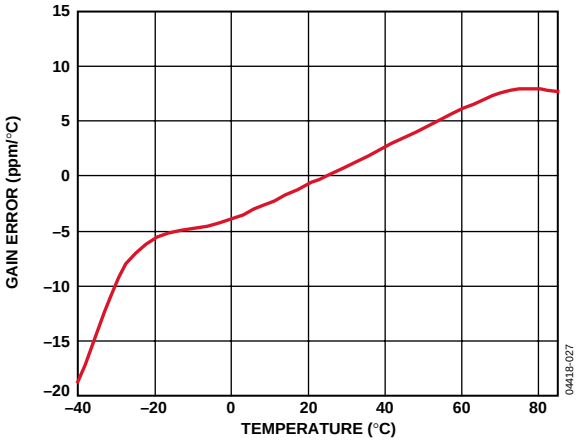

Figure 27. Gain Error vs. Temperature

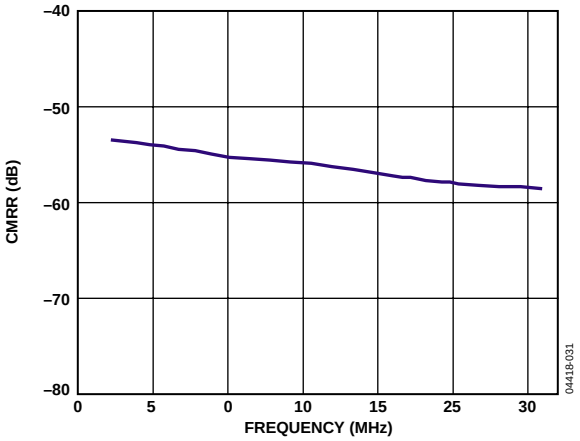

Figure 30. CMRR vs. Frequency, f_{SAMPLE} = 65 MSPS

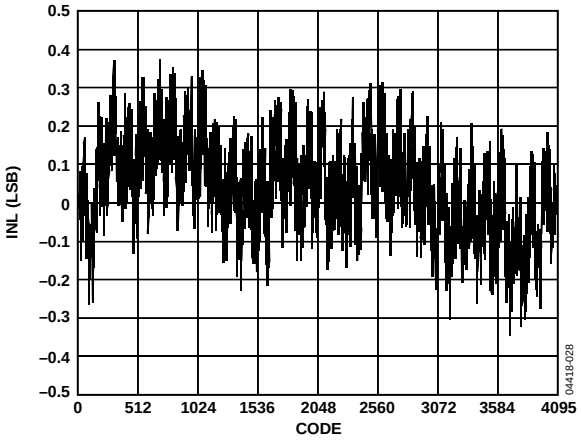

Figure 28. Typical INL, f_{IN} = 2.4 MHz, f_{SAMPLE} = 65 MSPS

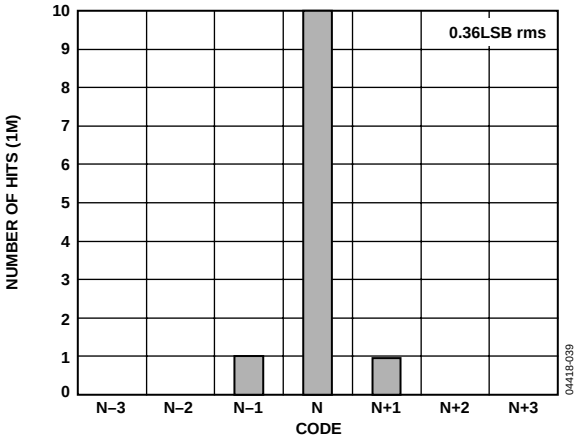

Figure 31. Input Referred Noise Histogram, f_{SAMPLE} = 65 MSPS

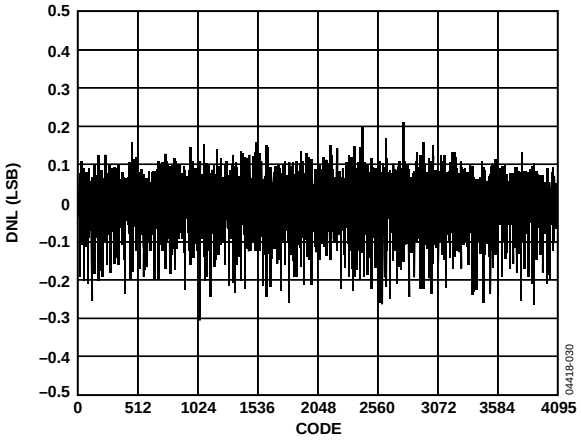

Figure 29. Typical DNL, f_{IN} = 2.4 MHz, f_{SAMPLE} = 65 MSPS

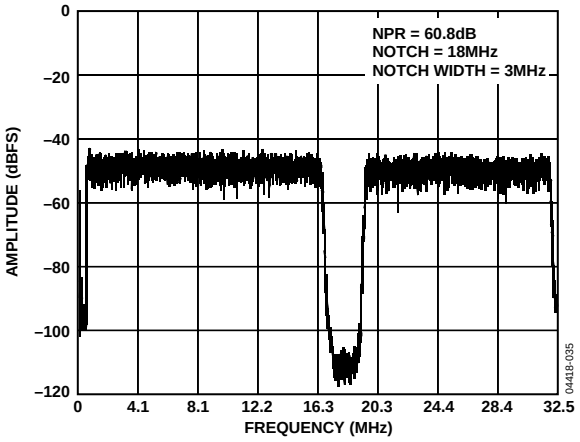

Figure 32. Noise Power Ratio (NPR), f_{SAMPLE} = 65 MSPS

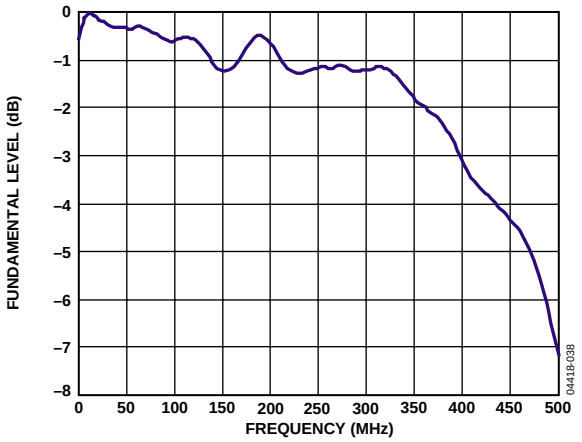

Figure 33. Full Power Bandwidth vs. Frequency, f_{SAMPLE} = 65 MSPS

TERMINOLOGY

Analog Bandwidth
Analog bandwidth is the analog input frequency at which the spectral power of the fundamental frequency (as determined by the FFT analysis) is reduced by 3 dB from full scale.

Aperture Delay
Aperture delay is a measure of the sample-and-hold amplifier (SHA) performance and is measured from the 50% point rising edge of the clock input to the time at which the input signal is held for conversion.

Aperture Uncertainty (Jitter)
Aperture jitter is the variation in aperture delay for successive samples and can be manifested as frequency-dependent noise on the ADC input.

Clock Pulse Width and Duty Cycle
Pulse width high is the minimum amount of time that the clock pulse should be left in the Logic 1 state to achieve rated performance. Pulse width low is the minimum time the clock pulse should be left in the low state. At a given clock rate, these specifications define an acceptable clock duty cycle.

Common Mode Rejection Ratio (CMRR)
CMRR is defined as the amount of rejection on the differential analog inputs when a common signal is applied. Typically expressed as 20 log (differential gain/common-mode gain).

Crosstalk
Crosstalk is defined as the measure of any feedthrough coupling onto the quiet channel when all other channels are driven by a full-scale signal.

Differential Analog Input Voltage Range
The peak-to-peak differential voltage that must be applied to the converter to generate a full-scale response. Peak differential voltage is computed by observing the voltage on a pin and subtracting the voltage from a second pin that is 180° out of phase. Peak-to-peak differential is computed by rotating the input phase 180° and taking the peak measurement again. The difference is computed between both peak measurements.

Differential Nonlinearity (DNL, No Missing Codes)
An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Guaranteed no missing codes to an n-bit resolution indicates that all 2^n codes, respectively, must be present over all operating ranges.

Effective Number of Bits (ENOB)
For a sine wave, SINAD can be expressed in terms of the number of bits. Using the following formula, it is possible to obtain a measure of performance expressed as *N*, the effective number of bits:

$$N = (\text{SINAD} - 1.76)/6.02$$

Full Power Bandwidth
Full power bandwidth is the measured –3 dB point at the analog front end input relative to the frequency measured.

Gain Error
The largest gain error is specified and is considered the difference between the measured and ideal full-scale input voltage range.

Gain Matching
Expressed in %FSR. Computed using the following equation:

$$GainMatching = \frac{FSR_{\max} - FSR_{\min}}{\left(\frac{FSR_{\max} + FSR_{\min}}{2}\right)} \times 100\%$$

where FSR_{MAX} is the most positive gain error of the ADCs, and FSR_{MIN} is the most negative gain error of the ADCs.

Input-Referred Noise
Input-referred noise is a measure of the wideband noise generated by the ADC core. Histograms of the output codes are created while a dc signal is applied to the ADC input. Input referred noise is calculated using the standard deviation of the histograms and presented in terms of LSB rms.

Integral Nonlinearity (INL)
INL refers to the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1 ½ LSB beyond the last code transition. The deviation is measured from the middle of each particular code to the true straight line.

Noise Power Ratio (NPR)
NPR is the full-scale rms noise power injected into the ADC versus the rejected band of interest (notch depth measured).

Offset Error
The largest offset error is specified and is considered the difference between the measured and ideal voltage at the analog input that produces the midscale code at the outputs.

Offset Matching
Expressed in mV. Computed using the following equation:

$$OffsetMatching = OFF_{MAX} - OFF_{MIN}$$

where OFF_{MAX} is the most positive offset error and OFF_{MIN} is the most negative offset error.

Out-of-Range Recovery Time
Out-of-range recovery time is the time it takes for the ADC to reacquire the analog input after a transient from 10% above positive full scale to 10% above negative full scale, or from 10% below negative full scale to 10% below positive full scale.

Output Propagation Delay
The delay between the clock logic threshold and the time when all bits are within valid logic levels.

Second and Third Harmonic Distortion
The ratio of the rms signal amplitude to the rms value of the second or third harmonic component, reported in dBc.

Signal-to Noise and Distortion (SINAD) Ratio
SINAD is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding the first six harmonics and dc. The value for SNR is expressed in decibels.

Spurious-Free Dynamic Range (SFDR)
SFDR is the difference in dB between the rms amplitude of the input signal and the peak spurious signal.

Temperature Drift
The temperature drift for offset error and gain error specifies the maximum change from the initial (25°C) value to the value at T_{MIN} or T_{MAX}.

Two-Tone SFDR
The ratio of the rms value of either input tone to the rms value of the peak spurious component. The peak spurious component may or may not be an IMD product. It may be reported in dBc (that is, degrades as signal levels are lowered) or in dBFS (always related back to converter full scale).

THEORY OF OPERATION

The AD9229 architecture consists of a front end switched capacitor sample-and-hold amplifier (SHA) followed by a pipelined ADC. The pipelined ADC is divided into three sections: a 4-bit first stage followed by eight 1.5-bit stages and a final 3-bit flash. Each stage provides sufficient overlap to correct for flash errors in the preceding stages. The quantized outputs from each stage are combined into a final 12-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate on a new input sample while the remaining stages operate on preceding samples. Sampling occurs on the rising edge of the clock.

Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC connected to a switched capacitor DAC and interstage residue amplifier (MDAC). The residue amplifier magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each stage to facilitate digital correction of flash errors. The last stage simply consists of a flash ADC.

The input stage contains a differential SHA that can be configured as ac- or dc-coupled in differential or single-ended modes. The output staging block aligns the data, carries out the error correction, and passes the data to the output buffers. The data is then serialized and aligned to the frame and output clock.

ANALOG INPUT CONSIDERATIONS

The analog input to the AD9229 is a differential-switched capacitor SHA that has been designed for optimum performance while processing a differential input signal. The SHA input can support a wide common-mode range and maintain excellent performance. An input common-mode voltage of mid-supply minimizes signal-dependent errors and provides optimum performance.

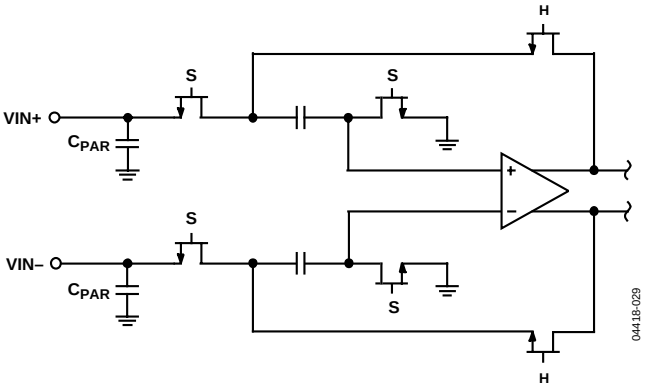

Figure 34. Switched-Capacitor SHA Input

The clock signal alternately switches the SHA between sample mode and hold mode (see Figure 34). When the SHA is switched into sample mode, the signal source must be capable of charging the sample capacitors and settling within one-half of a clock cycle. A small resistor in series with each input can help reduce the peak transient current required from the output stage of the driving source. Also, a small shunt capacitor can be placed across the inputs to provide dynamic charging currents. This passive network creates a low-pass filter at the ADC's input; therefore, the precise values are dependent on the application.

The analog inputs of the AD9229 are not internally dc-biased. In ac-coupled applications, the user must provide this bias externally. Setting the device so that $V_{CM} = AVDD/2$ is recommended for optimum performance, but the device functions over a wider range with reasonable performance (see Figure 35 and Figure 36).

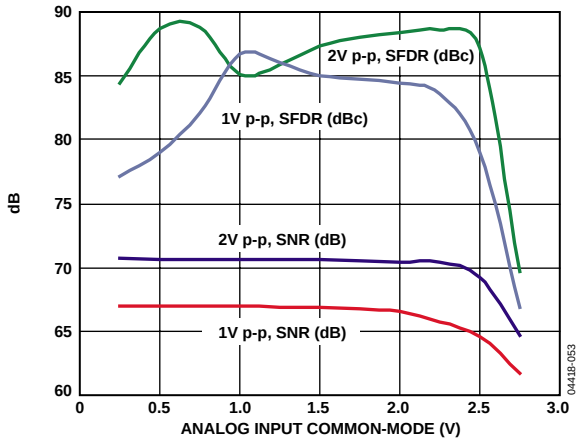

Figure 35. SNR, SFDR vs. Common-Mode Voltage, f_{IN} = 2.4 MHz, f_{SAMPLE} = 65 MSPS

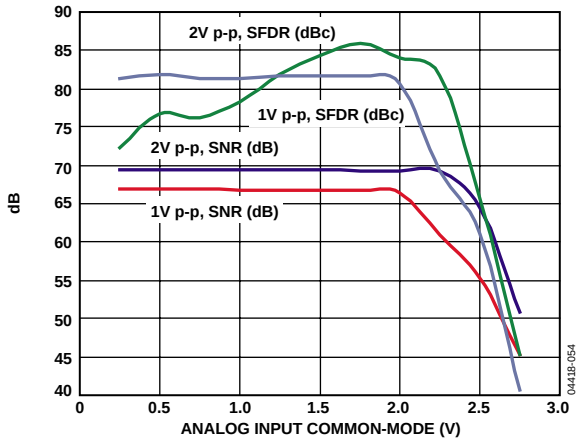

Figure 36. SNR, SFDR vs. Common-Mode Voltage, f_{IN} = 30 MHz, f_{SAMPLE} = 65 MSPS

For best dynamic performance, the source impedances driving VIN+ and VIN− should be matched such that common-mode settling errors are symmetrical. These errors are reduced by the common-mode rejection of the ADC.

An internal reference buffer creates the positive and negative reference voltages, REFT and REFB, respectively, that defines the span of the ADC core. The output common-mode of the reference buffer is set to midsupply, and the REFT and REFB voltages and span are defined as

$$REFT = 1/2\ (AVDD + VREF)$$
$$REFB = 1/2\ (AVDD - VREF)$$
$$Span = 2 \times (REFT - REFB) = 2 \times VREF$$

It can be seen from the equations above that the REFT and REFB voltages are symmetrical about the midsupply voltage and, by definition, the input span is twice the value of the VREF voltage.

The internal voltage reference can be pin-strapped to fixed values of 0.5 V or 1.0 V or adjusted within the same range, as discussed in the Internal Reference Connection section. Maximum SNR performance is achieved by setting the AD9229 to the largest input span of 2 V p-p.

The SHA should be driven from a source that keeps the signal peaks within the allowable range for the selected reference voltage. The minimum and maximum common-mode input levels are defined in Figure 35 and Figure 36.

Differential Input Configurations

Optimum performance is achieved by driving the AD9229 in a differential input configuration. For ultrasound applications, the AD8334 differential driver provides excellent performance and a flexible interface to the ADC (see Figure 37).

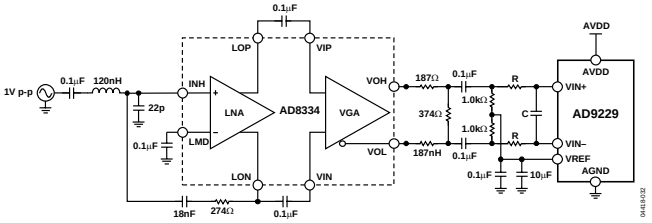

Figure 37. Differential Input Configuration Using the AD8334

However, the noise performance of most amplifiers is not adequate to achieve the true performance of the AD9229. For applications where SNR is a key parameter, differential transformer coupling is the recommended input configuration. An example of this is shown in Figure 38.

In any configuration, the value of the shunt capacitor, C, is dependent on the input frequency and may need to be reduced or removed.

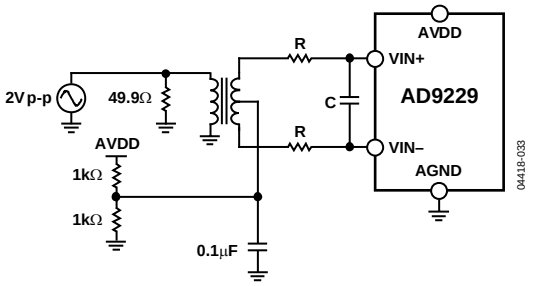

Figure 38. Differential Transformer—Coupled Configuration

Single-Ended Input Configuration

A single-ended input may provide adequate performance in cost-sensitive applications. In this configuration, SFDR and distortion performance degrade due to the large input common-mode swing. However, if the source impedances on each input are matched, there should be little effect on SNR performance. Figure 39 details a typical single-ended input configuration.

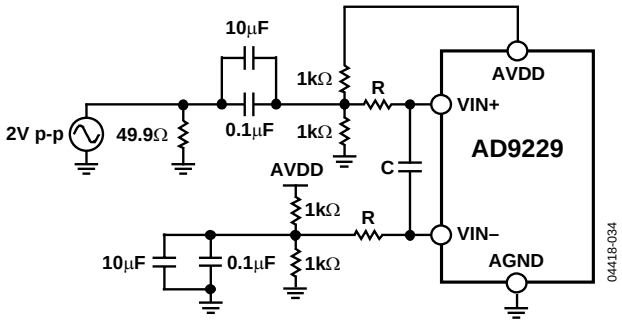

Figure 39. Single-Ended Input Configuration

CLOCK INPUT CONSIDERATIONS

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals, and as a result may be sensitive to clock duty cycle. Typically, a 10% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics. The AD9229 has a self-contained clock duty cycle stabilizer that retimes the nonsampling edge, providing an internal clock signal with a nominal 50% duty cycle. This allows a wide range of clock input duty cycles without affecting the performance of the AD9229.

An on-board phase-locked loop (PLL) multiplies the input clock rate for the purpose of shifting the serial data out. The stability criteria for the PLL limits the minimum sample clock rate of the ADC to 10 MSPS. Assuming steady state operation of the input clock, any sudden change in the sampling rate could create an out-of-lock condition leading to invalid outputs at the DCO, FCO, and data out pins.

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given full-scale input frequency (f_A) due only to aperture jitter (t_A) can be calculated with the following equation:

$$SNR\ degradation = 20 \times \log10\ [1/2 \times \pi \times f_A \times t_A]$$

In the equation, the rms aperture jitter, t_A, represents the root sum square of all jitter sources, which include the clock input, analog input signal, and ADC aperture jitter specification. Applications that require under-sampling are particularly sensitive to jitter.

The clock input should be treated as an analog signal in cases where aperture jitter may affect the dynamic range of the AD9229. Power supplies for clock drivers should be separated from the ADC output driver supplies to avoid modulating the clock signal with digital noise. Low jitter, crystal-controlled oscillators make the best clock sources. If the clock is generated from another type of source (by gating, dividing, or other methods), it should be retimed by the original clock at the last step.

Power Dissipation and Power-Down Mode

As shown in Figure 40 and Figure 41, the power dissipated by the AD9229 is proportional to its sample rate. The digital power dissipation does not vary much because it is determined primarily by the DRVDD supply and bias current of the LVDS output drivers.

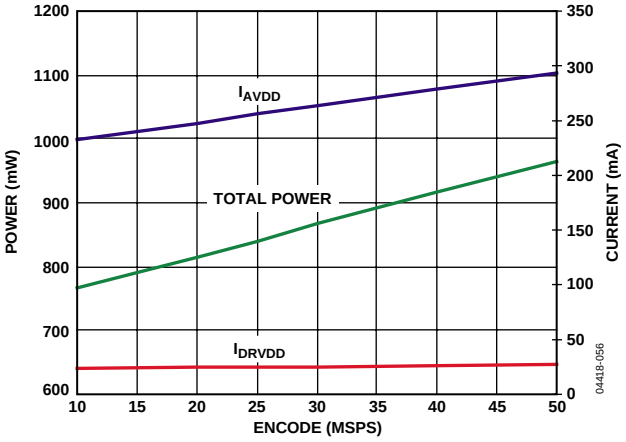

Figure 40. AD9229-50, Supply Current vs. f_{SAMPLE} for f_{IN} = 10.3 MHz

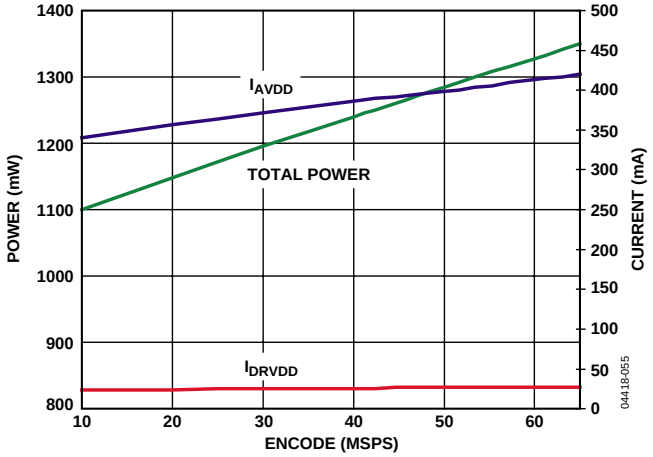

Figure 41. AD9229-65, Supply Current vs. f_{SAMPLE} for f_{IN} = 10.3 MHz

By asserting the PDWN pin high, the AD9229 is placed in power-down mode. In this state, the ADC typically dissipates 3 mW. During power down, the LVDS output drivers are placed in a high impedance state. Reasserting the PDWN pin low returns the AD9229 to normal operating mode.

In power-down mode, low power dissipation is achieved by shutting down the reference, reference buffer, PLL, and biasing networks. The decoupling capacitors on REFT and REFB are discharged when entering standby mode and then must be recharged when returning to normal operation. As a result, the wake-up time is related to the time spent in the power-down mode; shorter cycles result in proportionally shorter wake-up times. With the recommended 0.1 µF and 10 µF decoupling capacitors on REFT and REFB, it takes approximately 1 second to fully discharge the reference buffer decoupling capacitors and 4 ms to restore full operation.

Digital Outputs

The AD9229's differential outputs conform to the ANSI-644 LVDS standard. To set the LVDS bias current, place a resistor (RSET is nominally equal to 4.0 kΩ) to ground at the LVDSBIAS pin. The RSET resistor current is derived on-chip and sets the output current at each output equal to a nominal 3.5 mA. A 100 Ω differential termination resistor placed at the LVDS receiver inputs results in a nominal 350 mV swing at the receiver. To adjust the differential signal swing, simply change the resistor to a different value, as shown in Table 7.

Table 7. LVDSBIAS Pin Configuration

RSET	Differential Output Swing
3.7 kΩ	375 mV p-p
4.0 kΩ (Default)	350 mV p-p
4.3 kΩ	325 mV p-p

The AD9229's LVDS outputs facilitate interfacing with LVDS receivers in custom ASICs and FPGAs that have LVDS capability for superior switching performance in noisy environments. Single point-to-point net topologies are recommended with a 100 Ω termination resistor placed as close to the receiver as possible. It is recommended to keep the trace length no longer than 12 inches and to keep differential output traces close together and at equal lengths.

The format of the output data is offset binary. An example of the output coding format can be found in Table 8.

Table 8. Digital Output Coding

Code	(VIN+) – (VIN–), Input Span = 2 V p-p (V)	(VIN+) – (VIN–), Input Span = 1 V p-p (V)	Digital Output Offset Binary (D11 ... D0)
4095	1.000	0.500	1111 1111 1111
2048	0	0	1000 0000 0000
2047	−0.000488	−0.000244	0111 1111 1111
0	−1.00	−0.5000	0000 0000 0000

Timing

Data from each ADC is serialized and provided on a separate channel. The data rate for each serial stream is equal to 12 bits times the sample clock rate, with a maximum of 780 bps (12 bits × 65 MSPS = 780 bps). The lowest typical conversion rate is 10 MSPS.

Two output clocks are provided to assist in capturing data from the AD9229. The DCO is used to clock the output data and is equal to six times the sampling clock (CLK) rate. Data is clocked out of the AD9229 and can be captured on the rising and falling edges of the DCO that supports double-data rate (DDR) capturing. The frame clock out (FCO) is used to signal the start of a new output byte and is equal to the sampling clock rate. See the timing diagram shown in Figure 2 for more information.

DTP Pin

The digital test pattern (DTP) pin can be enabled for two different types of test patterns, as summarized in Table 9. When the DTP is tied to AVDD/3, all the ADC channel outputs shift out the following pattern: 1000 0000 0000. When the DTP is tied to 2 × AVDD/3, all the ADC channel outputs shift out the following pattern: 1010 1010 1010. The FCO and DCO outputs still work as usual while all channels shift out the test pattern. This pattern allows the user to perform timing alignment adjustments between the FCO, DCO, and the output data. For normal operation this pin should be tied to AGND.

Table 9. Digital Test Pattern Pin Settings

Selected DTP	DTP Voltage	Resulting D+ and D–	Resulting FCO and DCO
Normal Operation	AGND	Normal operation	Normal operation
DTP1	AVDD/3	1000 0000 0000	Normal operation
DTP2	2 × AVDD/3	1010 1010 1010	Normal operation
Restricted	AVDD	N/A	N/A

Voltage Reference

A stable and accurate 0.5 V voltage reference is built into the AD9229. The input range can be adjusted by varying the reference voltage applied to the AD9229, using either the internal reference or an externally applied reference voltage. The input span of the ADC tracks reference voltage changes linearly.

When applying the decoupling capacitors to the VREF, REFT, and REFB pins, use ceramic, low ESR capacitors. These capacitors should be close to the ADC pins and on the same layer of the PCB as the AD9229. The recommended capacitor values and configurations for the AD9229 reference pin can be found in Figure 42 and Figure 43.

Table 10. Reference Settings

Selected Mode	SENSE Voltage	Resulting VREF (V)	Resulting Differential Span (V p-p)
External Reference	AVDD	N/A	2 × external reference
Internal, 1 V p-p FSR	VREF	0.5	1.0
Programmable	0.2 V to VREF	0.5 × (1 + R2/R1)	2 × VREF
Internal, 2 V p-p FSR	AGND to 0.2 V	1.0	2.0

Internal Reference Connection

A comparator within the AD9229 detects the potential at the SENSE pin and configures the reference into four possible states (summarized in Table 10). If SENSE is grounded, the reference amplifier switch is connected to the internal resistor divider (see Figure 42), setting VREF to 1 V. Connecting the SENSE pin to the VREF pin switches the amplifier output to the SENSE pin, configuring the internal op amp circuit as a voltage follower and providing a 0.5 V reference output. If an external resistor divider is connected as shown in Figure 43, the switch is again set to the SENSE pin. This puts the reference amplifier in a noninverting mode and defines the VREF output as

$$VREF = 0.5 \times \left(1 + \frac{R2}{R1}\right)$$

In all reference configurations, REFT and REFB establish their input span of the ADC core. The analog input full-scale range of the ADC equals twice the voltage at the reference pin for either an internal or an external reference configuration.

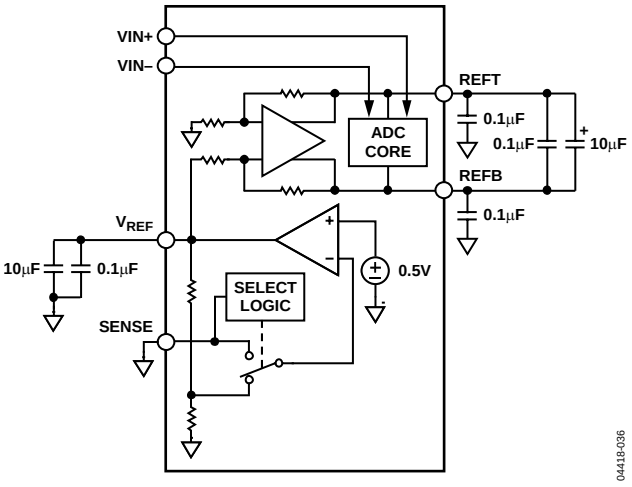

Figure 42. Internal Reference Configuration

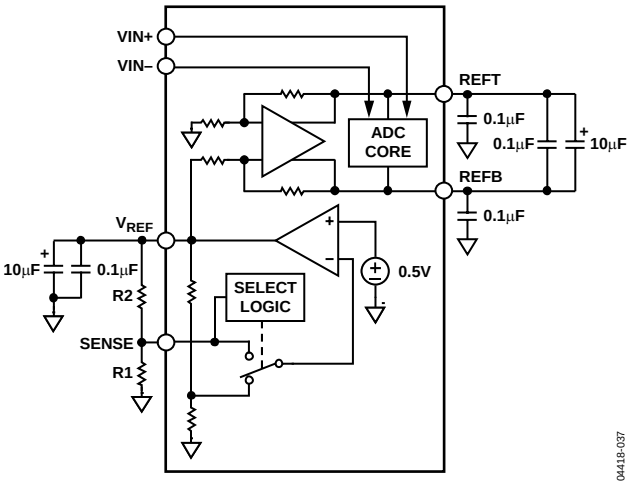

Figure 43. Programmable Reference Configuration

If the internal reference of the AD9229 is used to drive multiple converters to improve gain matching, the loading of the reference by the other converters must be considered. Figure 44 depicts how the internal reference voltage is affected by loading.

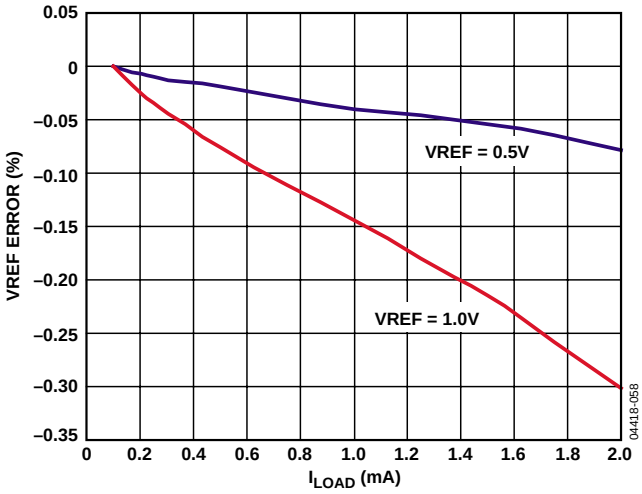

Figure 44. VREF Accuracy vs. Load

External Reference Operation

The use of an external reference may be necessary to enhance the gain accuracy of the ADC or improve thermal drift characteristics. Figure 45 shows the typical drift characteristics of the internal reference.

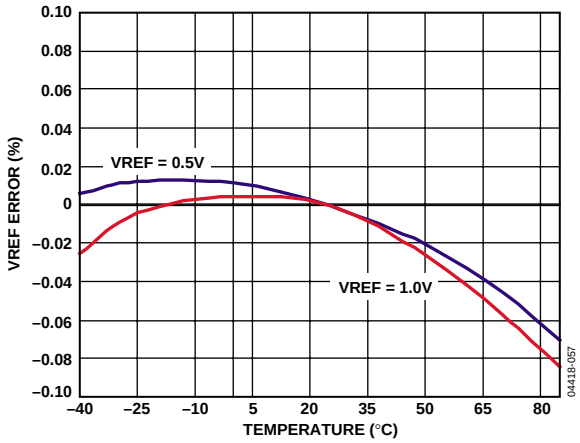

Figure 45. Typical VREF Drift

When the SENSE pin is tied to AVDD, the internal reference is disabled, allowing the use of an external reference. The external reference is loaded with an equivalent 7 kΩ load. An internal reference buffer generates the positive and negative full-scale references, REFT, and REFB for the ADC core. Therefore, the external reference must be limited to a maximum of 1 V.

Power and Ground Recommendations

When connecting power to the AD9229, it is recommended that two separate 3.0 V supplies be used: one for analog (AVDD) and one for digital (DRVDD). If only one supply is available, then it should be routed to the AVDD first and tapped off and isolated with a ferrite bead or filter choke with decoupling capacitors proceeding. The user can employ several different decoupling capacitors to cover both high and low frequencies. These should be located close to the point of entry at the PC board level and close to the parts with minimal trace length.

A single PC board ground plane should be sufficient when using the AD9229. With proper decoupling and smart partitioning of the PC board's analog, digital, and clock sections, optimum performance is easily achieved.

Exposed Paddle Thermal Heat Slug Recommendations

It is mandatory that the exposed paddle on the underside of the ADC is connected to analog ground (AGND) to achieve the best electrical and thermal performance of the AD9229. A continuous exposed (no solder mask) copper plane on the PCB should mate to the AD9229 exposed paddle, Pin 0. The copper plane should have several vias to achieve the lowest possible resistive thermal path for heat dissipation to flow through the bottom of the PCB. These vias should be solder filled or plugged.

To maximize the coverage and adhesion between the ADC and PCB, overlay a silkscreen to partition the continuous plane on the PCB into several uniform sections. This provides several tie points between the two during the reflow process. Using one continuous plane with no partitions only guarantees one tie point between the ADC and PCB. See Figure 46 for a PCB layout example. For detailed information on packaging and the PCB layout of chip scale packages, go to www.analog.com.

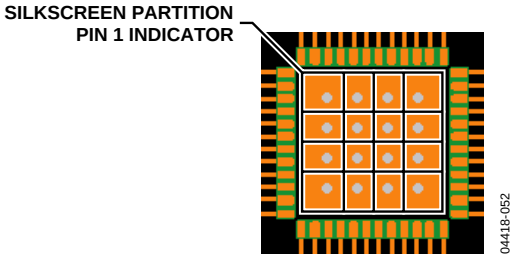

Figure 46. Typical PCB Layout

EVALUATION BOARD

The AD9229 evaluation board provides all of the support circuitry required to operate the ADC in its various modes and configurations. The converter can be driven differentially through a transformer (default) or through the AD8334 driver. The ADC can also be driven single-ended. Separate power pins are provided to isolate the DUT from the support circuitry. Each input configuration can be selected by proper connection of various jumpers (see Figure 48 to Figure 51). Figure 47 shows the typical bench characterization setup used to evaluate the ac performance of the AD9229. It is critical that the signal sources used for the analog input and clock have very low phase noise (< 1 ps rms jitter) to realize the ultimate performance of the converter. Proper filtering of the analog input signal to remove harmonics and lower the integrated or broadband noise at the input is also necessary to achieve the specified noise performance.

See Figure 47 to Figure 57 for complete schematics and layout plots that demonstrate the routing and grounding techniques that should be applied at the system level.

POWER SUPPLIES

When operating the evaluation board in its default condition, at least one 3.0 V supply is needed with a 2 A current capability. It is recommended that separate supplies be used for both analog and digital. To use the deserialization board (HSC-ADC-FPGA2) and FIFO (HSC-ADC-EVALA-DC) data capture board with this setup, a separate 3.3 V supply is needed with a 2 A capability. To operate the evaluation board using the VGA option, a separate 5.0 V analog supply is needed in addition to the other 3.0 V and 3.3 V supplies. The 5.0 V supply should have a 1 A current capability.

INPUT SIGNALS

When connecting the clock and analog source, use clean signal generators with low phase noise. We recommend using Rohde & Schwarz SMHU or HP8644 signal generators or equivalent. Use 1 m long, shielded, 50 Ω coaxial cable for making connections to the evaluation board. Dial in the desired frequency set forth in the specifications tables and set the amplitude. Typically, most ADI evaluation boards can accept a 3 V p-p or 13 dBm sine wave input for the clock. When connecting the analog input source, we recommend a multipole, narrow-band band-pass filter with 50 Ω terminations. ADI uses TTE, Allen Avionics, and K and L type band-pass filters. The filter should be directly connected to the evaluation board if possible.

OUTPUT SIGNALS

In this particular setup, the HSC-ADC-FPGA2 high-speed deserialization board is used to deserialize the digital output data and convert it to parallel CMOS. Two channels that interface with ADI's standard dual channel FIFO data capture board (HSC-ADC-EVALA-DC) can be evaluated at the same time. For more information on these boards and their optional settings, see the analog website at www.analog.com/FIFO.

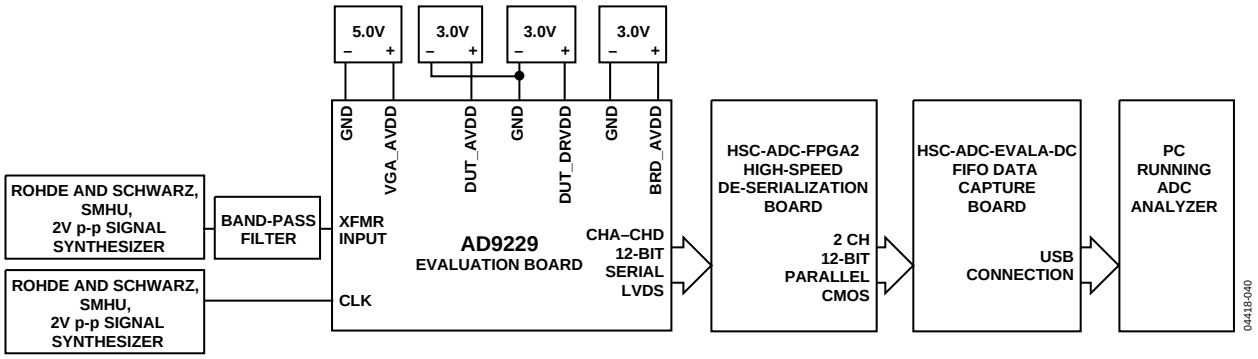

Figure 47. Evaluation Board Connections

DEFAULT OPERATION AND JUMPER SELECTION SETTINGS

The following is a list of the default and optional settings or modes allowed on the AD9229 evaluation board.

- Power: Three separate 3.0 V supply voltages are recommended to bias the ADC's analog and digital sections and the rest of the evaluation boards external support circuitry. However, by tying JP1, JP2, and JP4 together, the user can use a single 3.0 V supply to power the board in its default configuration.
- AIN: The evaluation board is setup for a transformer coupled analog input with optimum 50 Ω impedance matching out to 100 MHz. For more bandwidth response, the 20 pF differential capacitor across the analog input should be changed or removed. The common-mode of the analog inputs is developed from the center tap of the transformer. Other options on the analog input include driving multiple channels from a single source by tying JP18 through JP21, and JP24 through JP29 jumpers together in the configuration desired.
- VREF: VREF is set to 1.0 V by tying the SENSE pin to ground. This causes the ADC to operate in 2.0 V p-p full-scale range. A number of other VREF options are available on the evaluation board, including 1.0 V p-p full-scale range and a separate external reference option using the ADR510. To use these optional VREF modes, simply switch the jumper setting on U17. Proper use of the VREF options is noted in the Voltage Reference section.
- CLOCK: The clock input circuitry is derived from a simple logic circuit using a high-speed inverter that adds a very low amount of jitter to the clock path. The clock input is 50 Ω terminated and ac-coupled to handle sine wave type inputs.
- PWDN: To enable the power-down feature, simply short JP1 to AVDD on the PWDN pin.
- DTP: To enable either one of the digital test patterns on digital outputs of the ADC, tie a 1.0 V source to TP10 to enable test pattern 1000 0000 0000. If a 2.0 V source is tied to the DTP pin, then the following test pattern is enabled: 1010 1010 1010. Also, see the DTP Pin section for more details.
- LVDSBIAS: To change the level of the LVDS output level swing, simply change the value of R74. Other recommended values can be found in the Digital Outputs section.
- D+, D–: If an alternate data capture method to the setup described in Figure 49 is used, optional receiver terminations can be installed next to the high-speed backplane connector.

ALTERNATE ANALOG INPUT DRIVE CONFIGURATION

The following is a brief description of the alternate analog input drive configuration using the AD8334 quad VGA. This particular drive option may need to be populated, in which case all the necessary components are listed in the bill of material below. This section lists the necessary settings to properly configure the evaluation board for this option. For more details on the AD8334 quad VGA, how it works, and its optional pin settings, consult the AD8334 datasheet.

To configure the analog input to drive the VGA instead of the default transformer option, the following components need to be removed and/or changed.

1. Add a 5.0 V supply to the power connector header block that has a current capability of 1 A.
2. Remove R15, R30, R42, and R83, and T1, T2, T3, and T4 in the default analog input path.
3. Populate R62, R63, R64, and R65 with 0 Ω resistors in the analog input path.
4. Populate R29, R41, R70, R69, R66, R68, R73, and R72 with 0 Ω resistors to provide an input common-mode level to the analog input.
5. Populate JP6, JP7, JP12, JP15, JP16, JP23, JP30, and JP32 with solder shorts in the analog input path.

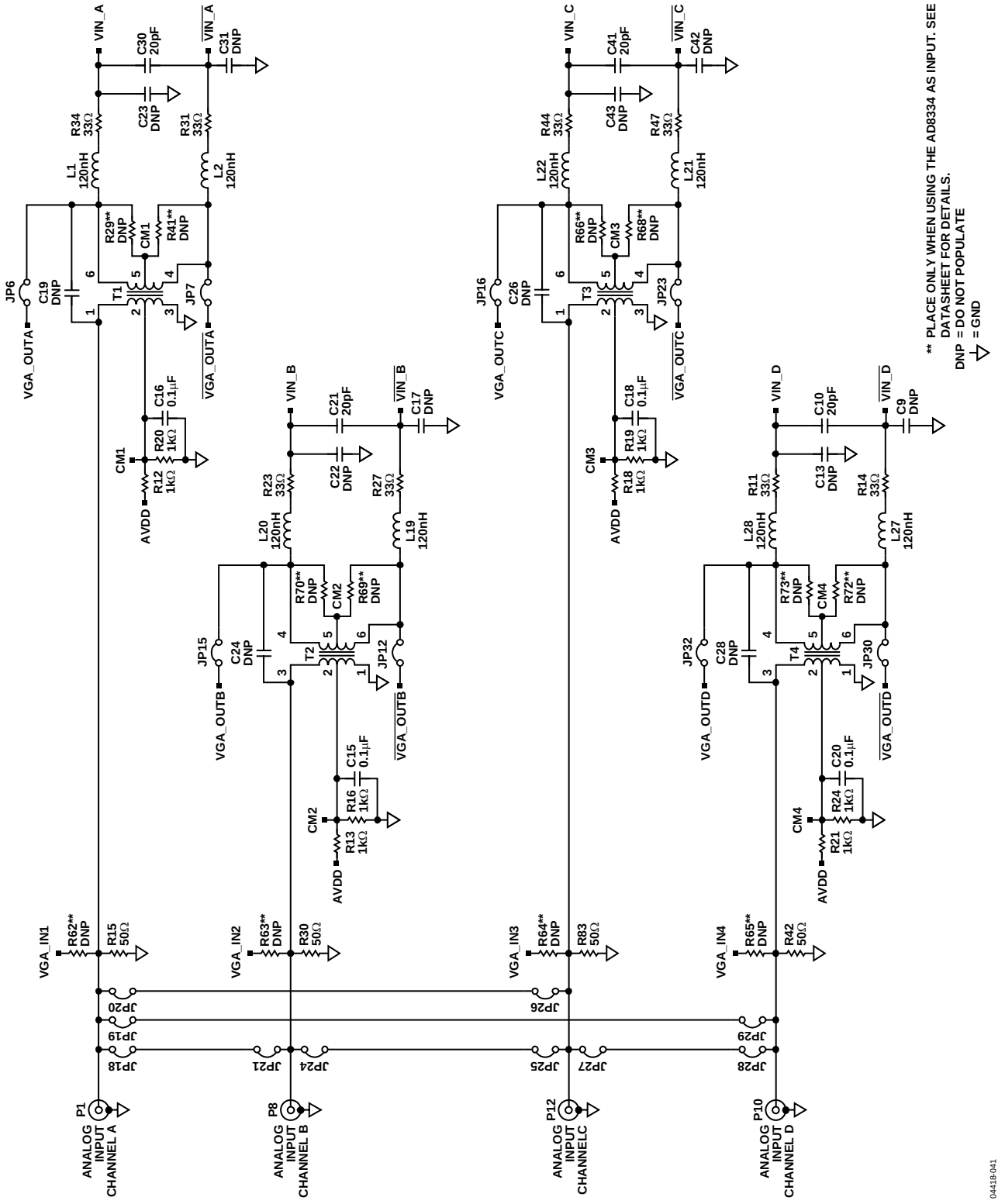

Figure 48. Evaluation Board Schematic, DUT Analog Input

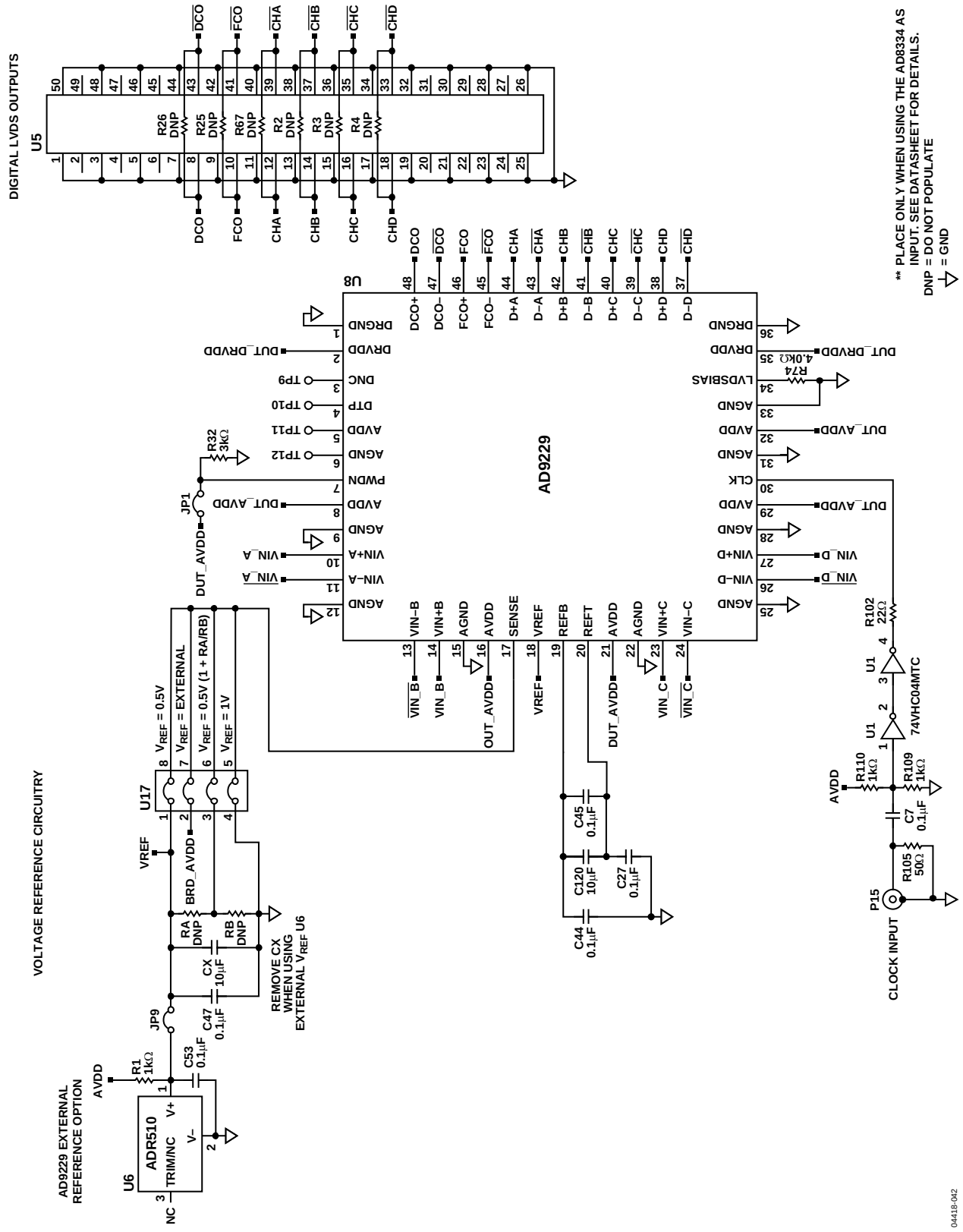

Figure 49. Evaluation Board Schematic, DUT, VREF, and Clock Inputs

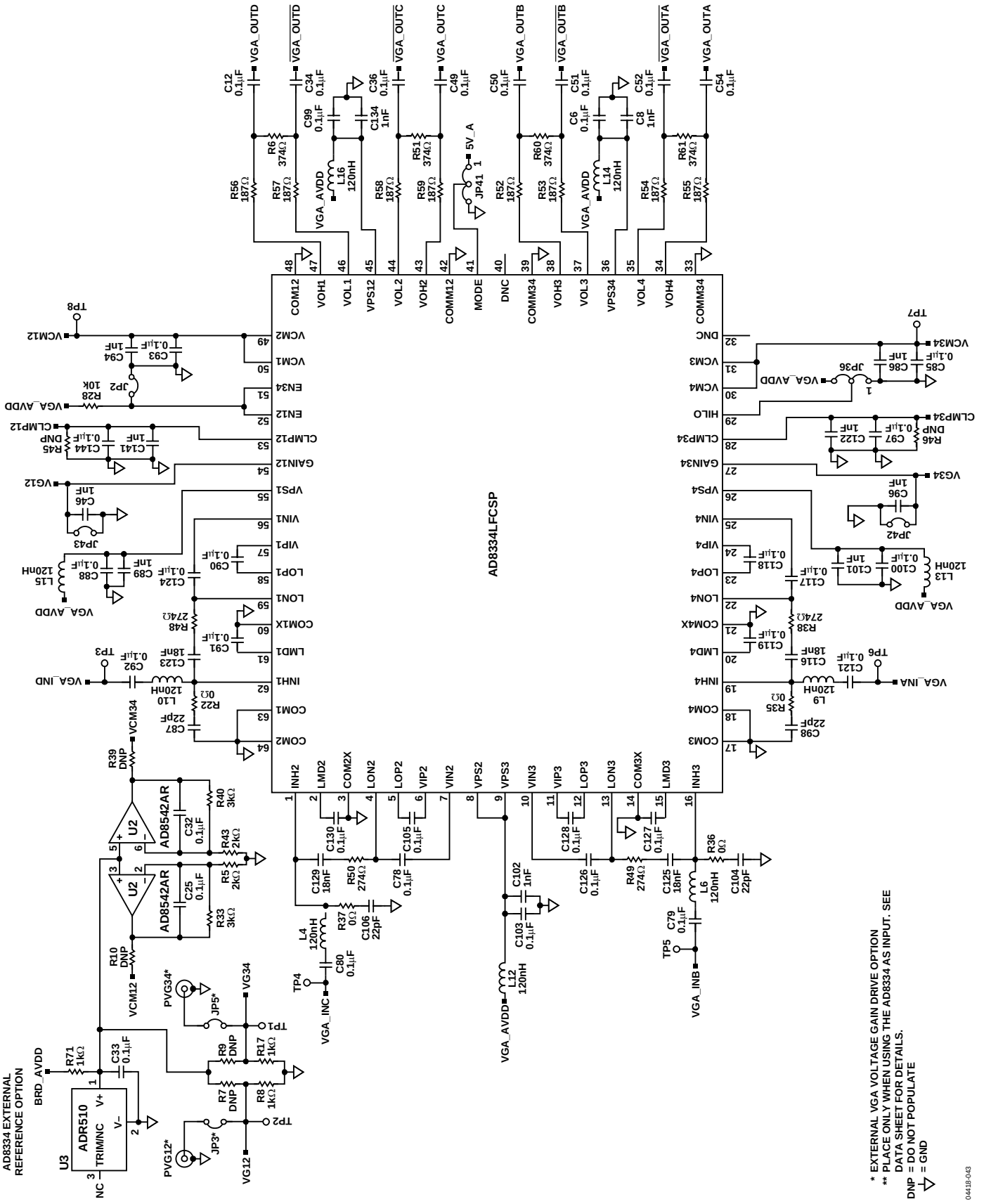

Figure 50. Evaluation Board Schematic, Optional DUT Analog Input Drive

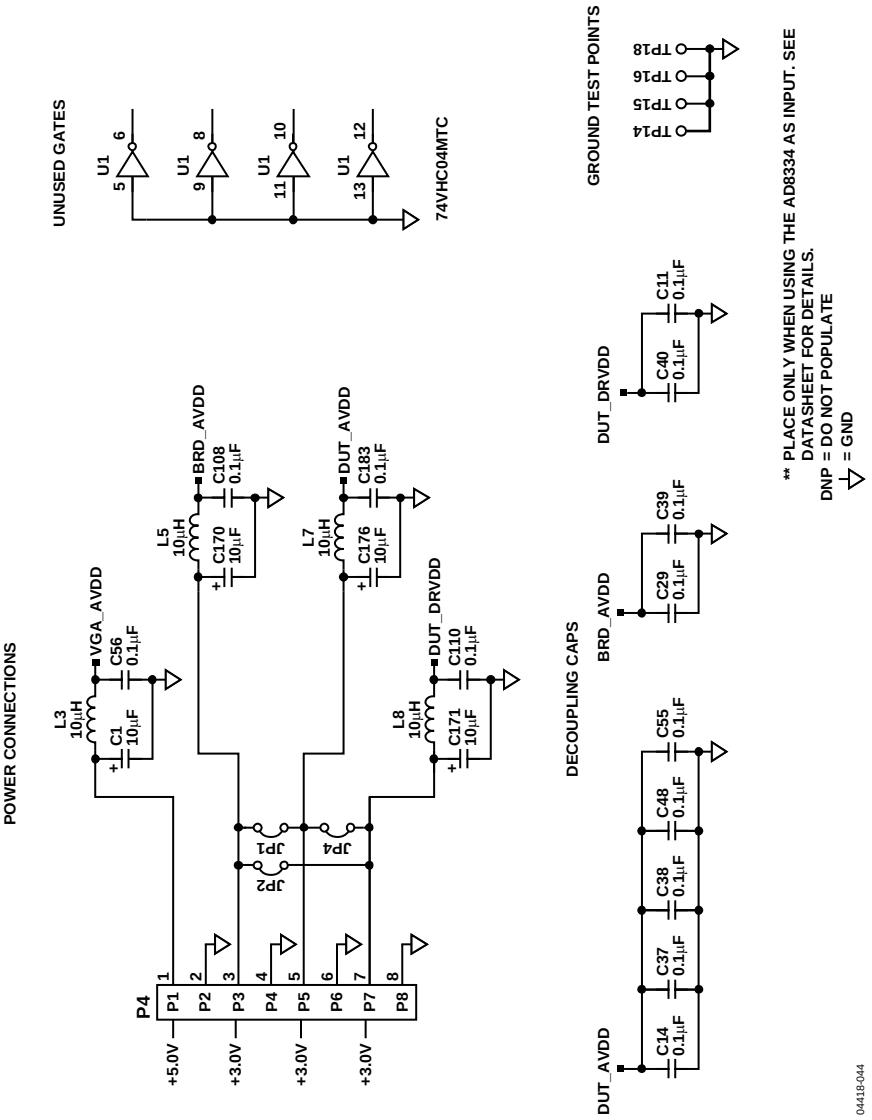

Figure 51. Evaluation Board Schematic, Power and Decoupling

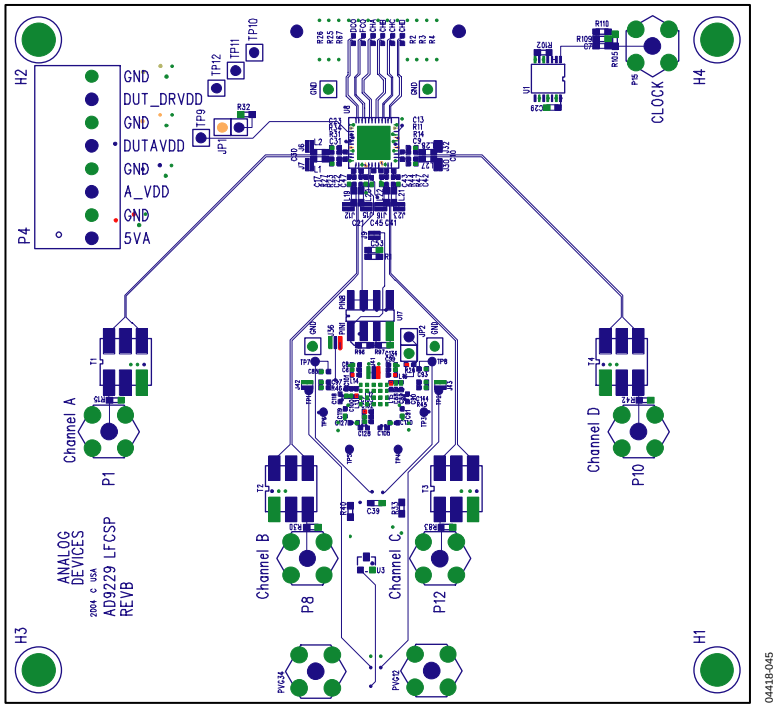

Figure 52. Evaluation Board Layout, Primary Side

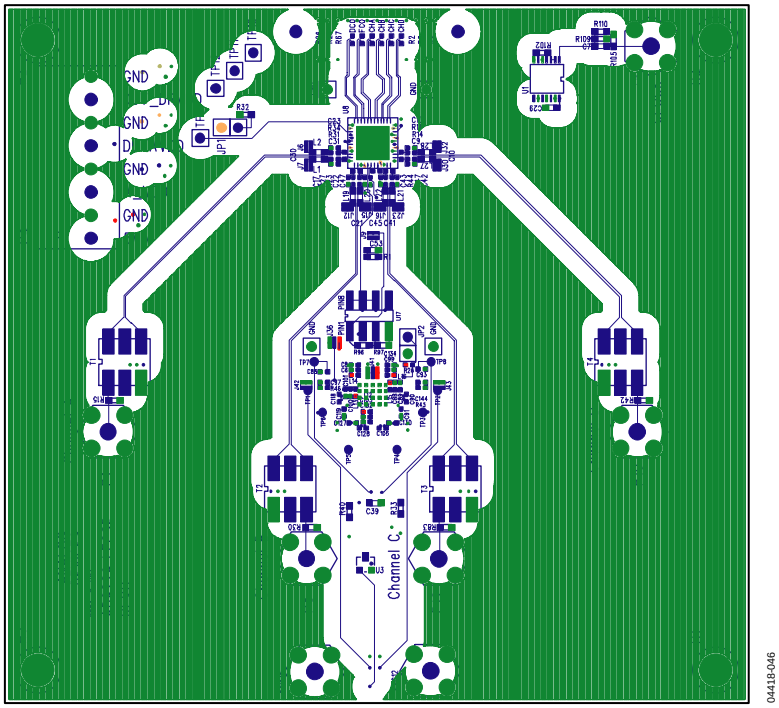

Figure 53. Evaluation Board Layout, Primary Side (With Ground Copper Pour)

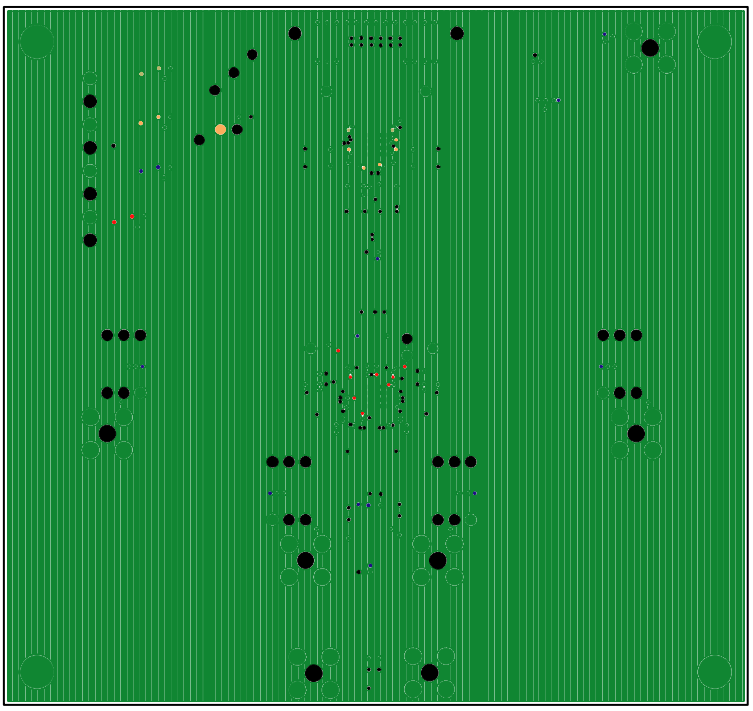

Figure 54. Evaluation Board Layout, Ground Plane

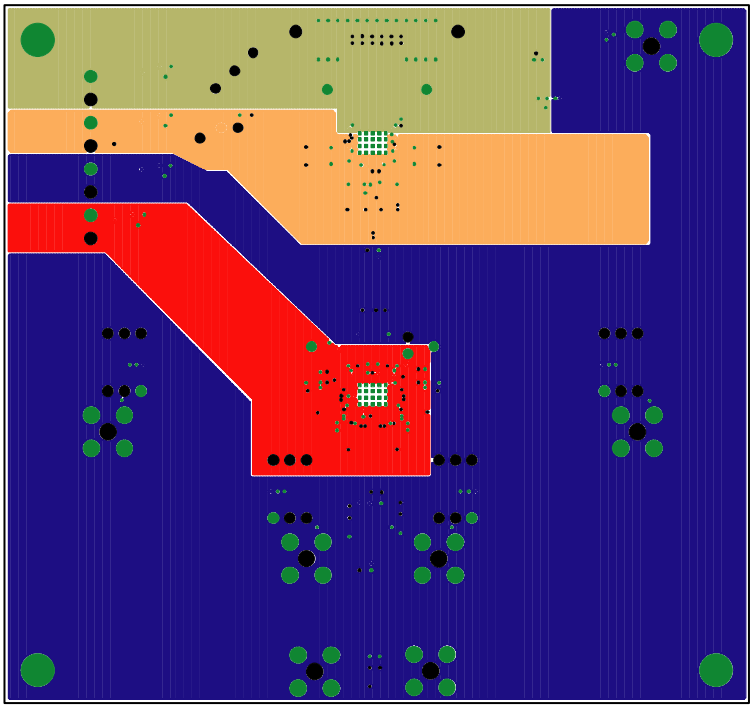

Figure 55. Evaluation Board Layout, Power Plane

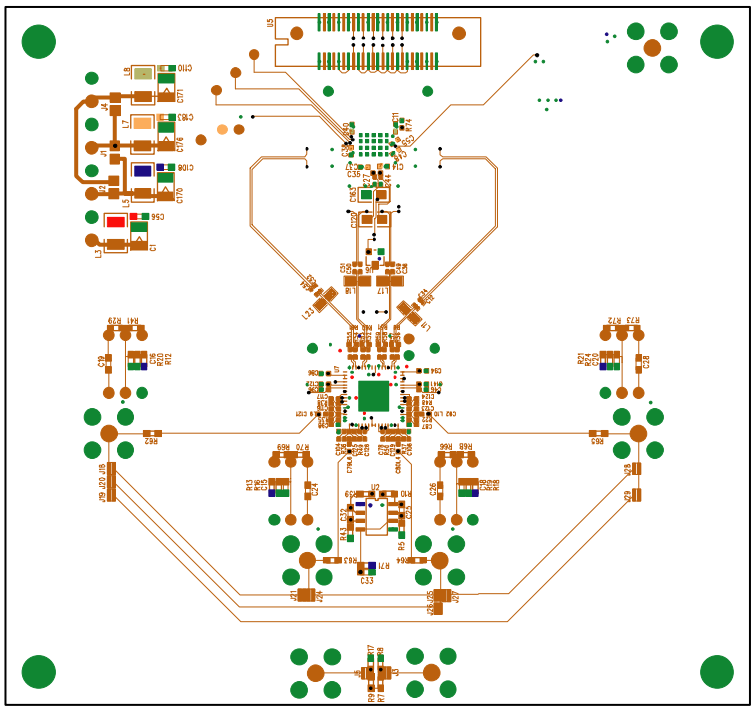

Figure 56. Evaluation Board Layout, Secondary Side

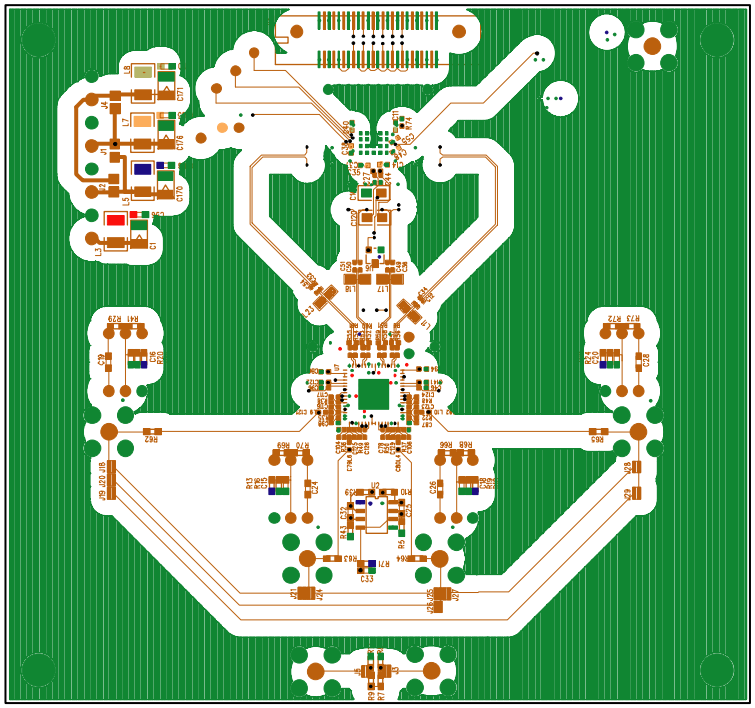

Figure 57. Evaluation Board Layout, Secondary Side (With Ground Copper Pour)

Table 11. Evaluation Board Bill of Materials (BOM)

Item	Qnty. per Board	REFDES	Device	Pkg.	Value	Mfg.	Mfg. Part Number
1	1	AD9229LFCSP_REVB	PCB	PCB	PCB		
2	4	R22, R35, R36, R37	Resistor	402	Resistor 0.0 Ω 1/16 W 5% 0402 SMD	Yageo America	9C04021A0R00JLHF3
3	8	R11, R14, R23, R27, R31, R34, R44, R47	Resistor	402	Resistor 33 Ω 1/16 W 5% 0402 SMD	Susumu Co Ltd	RR0510R-330-D
4	8	R52, R53, R54, R55, R56, R57, R58, R59	Resistor	402	Resistor 180 Ω 1/16 W 5% 0402 SMD	Susumu Co Ltd	RR0510P-181-D
5	4	R38, R48, R49, R50	Resistor	402	Resistor 270 Ω 1/16 W 5% 0402 SMD	Susumu Co Ltd	RR0510P-271-D
6	4	R6, R51, R60, R61	Resistor	402	Resistor 360 Ω 1/16 W 5% 0402 SMD	Susumu Co Ltd	RR0510P-361-D
7	1	R74	Resistor	402	Resistor 3.6 kΩ 1/16 W 5% 0402 SMD	Susumu Co Ltd	RR0510P-362-D
8	3	R28, R45, R46	Resistor	402	Resistor. 10.0 kΩ 1/16 W 5% 0402 SMD	Susumu Co Ltd	RR0510P-103-D
9	4	R62, R63, R64, R65	Resistor	603	Resistor 0.0 Ω 1/10 W 5% 0603 SMD	Yageo America	9C06031A0R00JLHFT
10	1	R102	Resistor	603	Resistor 22 Ω 1/16 W 5% 0603 SMD	Susumu Co Ltd	RR0816Q-220-D
11	5	R15, R30, R42, R83, R105	Resistor	603	Resistor 49.9 Ω 1/16 W 5% 0603 SMD	Susumu Co Ltd	RR0816Q-49R9-D-68R
12	24	R1, R7, R8, R9, R12, R13, R16, R17, R18, R19, R20, R21, R24, R29, R41, R66, R68, R69, R70, R71, R72, R73, R109, R110	Resistor	603	Resistor 1.0 kΩ 1/10 W 5% 0603 SMD	Panasonic—sECG	ERJ-3GEY0R00V
13	2	R5, R43	Resistor	603	Resistor 2.0 kΩ 1/10 W 5% 0603 SMD	Yageo America	9C06031A2001JLHFT
14	3	R32, R33, R40	Resistor	603	Resistor 3.0 kΩ 1/10 W 5% 0603 SMD	Panasonic—ECG	ERJ-3GEYJ302V
15	8	C10, C21, C30, C41, C87, C98, C104, C106	Capacitor	402	Capacitor 22 pF 50 V ± 5% Ceramic NP0 0402	Yageo America	0402CG220J9B200
16	11	C8, C46, C86, C89, C94, C96, C101, C102, C122, C134, C141	Capacitor	402	Capacitor 1000 pF 25 V ± 10% Ceramic X7R 0402	Kemet	C0402C102K3RACTU
17	4	C116, C123, C125, C129	Capacitor	402	Capacitor 18000 pF 6.3 V ± 10% Ceramic X5R 0402	Kemet	C0402C183K9PACTU
18	43	C6, C11, C12, C14, C27, C34, C35, C36, C37, C38, C40, C44, C45, C47, C48, C49, C50, C51, C52, C54, C55, C78, C79, C80, C85, C88, C90, C91, C92, C93, C97, C99, C100, C103, C105, C117, C118, C119, C121, C124, C126, C127, C128, C130, C144	Capacitor	402	Capacitor 0.1 µF 16 V +80/–20% Ceramic Y5V 0402	Panasonic—ECG	ECJ-0EF1C104Z
19	15	C7, C15, C16, C18, C20, C25, C29, C32, C33, C39, C53, C56, C108, C110, C183	Capacitor	603	Capacitor 0.10 µF 16 V ± 10% Ceramic X7R 0603	Yageo America	06032R104K7B20D
20	4	C19, C24, C26, C28	Capacitor	603	Do Not Populate (DNP)		
21	2	C120, C163	Capacitor	805	Capacitor 10 µF 6.3 V ± 10% Ceramic X5R 0805	AVX	08056D106KAT2A
22	4	C1, C170, C171, C176	Capacitor	1206	Capacitor, tantalum 10 µF 16 V 10% SMD	Kemet	T491B106K016AS
23	9	L4, L6, L9, L10, L12, L13, L14, L15, L16	Inductor	402	120 nH chip EMI filter, surface mount, 0402, 75 Ω ± 25% impedance (at 100 MHz), 100 mA	Murata	BLM15BB750PN1D
24	8	L1, L2, L19, L20, L21, L22, L27, L28	Capacitor	603	120 nH chip EMI filter, surface mount, 0603, 75 Ω ± 25%	Murata	BLM18BB750SN1D

Item	Qnty. per Board	REFDES	Device	Pkg.	Value	Mfg.	Mfg. Part Number
					impedance (at 100 MHz), 100 mA		
25	4	L11, L17, L18, L23	Inductor	805	120 nH chip EMI filter, surface mount, 0805, 75 Ω ± 25% impedance (at 100 MHz), 100 mA	Murata	BLM21BB750SN1D
26	4	L3, L5, L7, L8	Ferrite Bead	1210	Bead Core 3.2X2.5X1.6 SMD	Panasonic—ECG	EXC-CL3225U1
27	1	U5	Connector	SMT	FCN_268M01	Fujitsu	FCN-268M012-G/1D
28	1	U17	Header	2MMSMT-872	WM18158-ND	Molex/Waldom Electronics Corp	87267-0850
29	4	T1, T2, T3, T4	Transformer	SMT	ADT1-1WT	Minicircuits	ADT1-1WT
30	7	P1, P8, P10, P12, P15, PVG12, PVG34	SMA	Through hole	SMA	Amphenol-RF Division	901-144-8RFX
31	2	MH1, MH2	11/4" Standoff	Nylon	1 1/4" 6-32	RAF	4046-632-N
32	2	MH3, MH4	6-32 Nuts	Nylon	6-32	RAF	30528-N
33	1	P4-A	Header	8-pole PCB Header	Z5.531.3825.0 (Wieland)	Wieland	Z5.531.3825.0
34	1	P4-B	PWR Block	8-pole PCB Connector	25.600.5853.0 (Wieland)	Wieland	25.600.5853.0
35	1	JP1, JP2	SGLJMPR	Through Hole	TSW-120-07-G-S	Samtec	TSW-120-07-G-S
36	1	U1	Inverter	TSSOP-14	74VHC04MTC	Fairchild Semiconductor	74VHC04MTC
37	1	U7	Quad VGA	LFCSP	AD8334ACPZ	ADI	AD8334ACPZ
38	1	U8	Quad ADC	LFCSP	AD9229BCPZ-65	ADI	AD9229BCPZ-65
39	1	U2	Op Amp	SOIC-8	AD8542AR	ADI	AD8542AR
40	2	U3, U6	Reference	SOT23	ADR510ART	ADI	ADR510ART

OUTLINE DIMENSIONS

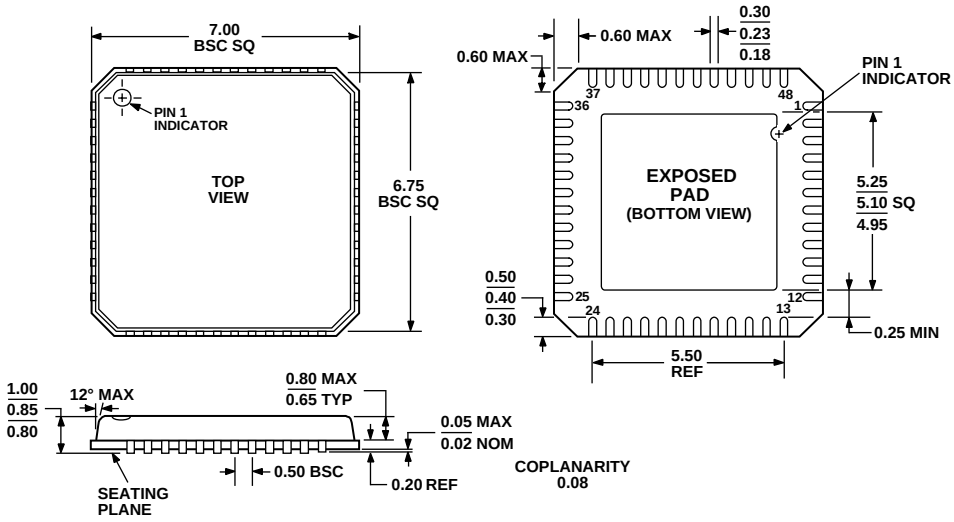

Figure 58. 48-Lead Frame Chip Scale Package [LFCSP]
(CP-48-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9229BCPZ-65[1]	–40°C to +85°C	48-Lead LFCSP	CP-48-1
AD9229BCPZRL7-65[1]	–40°C to +85°C	48-Lead LFCSP	CP-48-1
AD9229BCPZ-50[1]	–40°C to +85°C	48-Lead LFCSP	CP-48-1
AD9229BCPZRL7-50[1]	–40°C to +85°C	48-Lead LFCSP	CP-48-1
AD9229-65EB		Evaluation Board	

[1] Z=Pb-free part.

NOTES

D04418-0-3/05(0)